

Procedure Calling

- parameter placing in registers
- transfer control to procedure
- acquire storage for procedure
- perform procedure's operations
- place result in register for caller
- return to place of call

Few Registers

parameter passing → \$a0 - \$a3
returning results → \$v0 - \$v1
return address → \$ra

Others

\$t0 - \$t7, \$s0 - \$s7

\$gp → global pointer for static data

\$sp → stack pointer

Procedure calling in MIPS

jal procedureAddress



Jump-And-Link

link → put the address of the following instruction in \$ra

jump → jumps to target address

Returning from procedures in MIPS

jr \$ra



Jump Register

So, what we do is, (for procedures)

→ put parameters in $\$a0 - \$a3$ (caller)

→ $\boxed{\text{jal } X}$ to call procedure, X (callee)

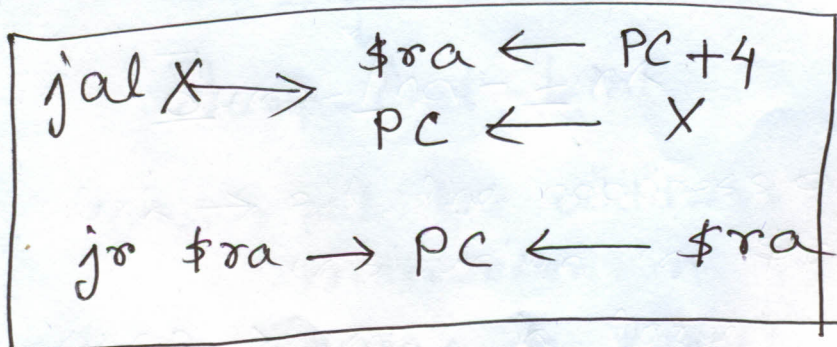
→ X computes results and put them in $\$v0 - \$v1$ (callee)

→ X then return control to the caller using $\text{jr } \$ra$

For all these work to do, procedure calling & jump/branch, we need to have a register to hold the address of the current instruction being executed. This register.

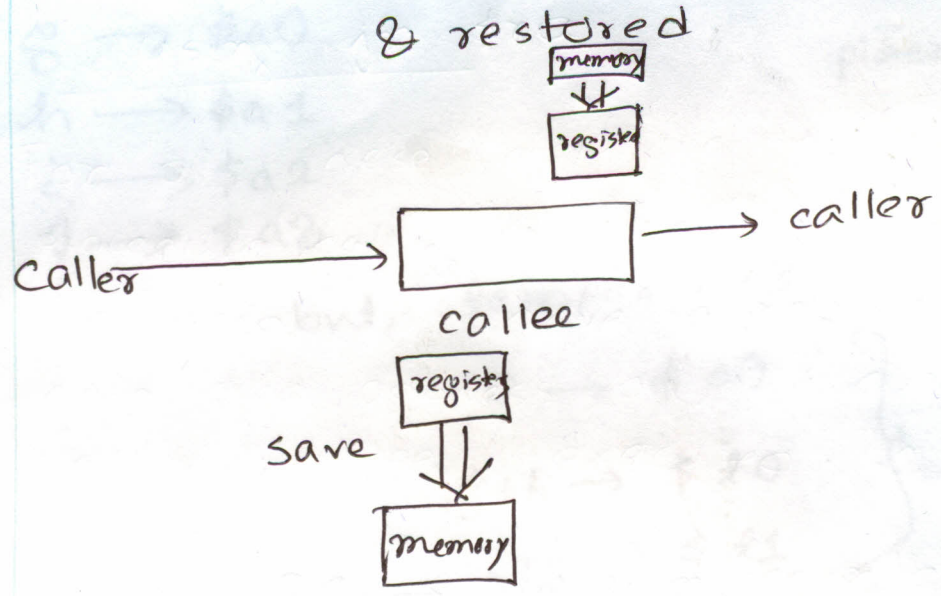
PC → program counter

also known as IAR → Instruction Address Register.

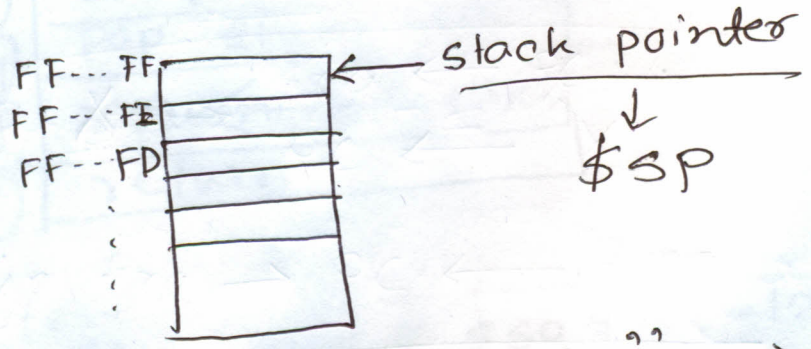


* Restoring Registers :

- procedure may need other registers apart from four parameter registers & two return value registers
- if other registers are used, their values must be saved & restored



- for this purpose we use stack (last-in-first-out) memory



```
"push" -> $SP--;  
"pop" -> $SP++;
```


int test (int g, int h, int i, int j) {

int f;

f = (g + h) - (i + j);

return f;

}

g → \$a0

h → \$a1

i → \$a2

j → \$a3

place result in
\$v0

but, temporaries,

f → \$s0

g+h → \$t0

i+j → \$t1

3 - push
to stack

1	sp ← sp - (3 * 4)
2	push them all
3	compute
4	pop them all
5	return sp + (3 * 4)
6	return

test:

1

addi \$sp, \$sp, -12

2

sw \$t1, 8(\$sp)
sw \$t0, 4(\$sp)
sw \$s0, 0(\$sp)

3

add \$t0, \$a0, \$a1
add \$t1, \$a2, \$a3
add \$s0, \$t0, \$t1
add \$v0, \$s0, \$zero

not completed

* Recap:

- Steps in procedure calling:

1. parameter register, $\boxed{\$a0 - \$a3}$
2. goto procedure, $\boxed{\text{j}al \text{ procLabel}}$
3. Acquire storage; $\boxed{\text{stack}}$
4. procedure operations
5. return result register, $\boxed{\$v0 - \$v1}$
6. return to place of call, $\boxed{\text{j}r \ \$ra}$

C-code

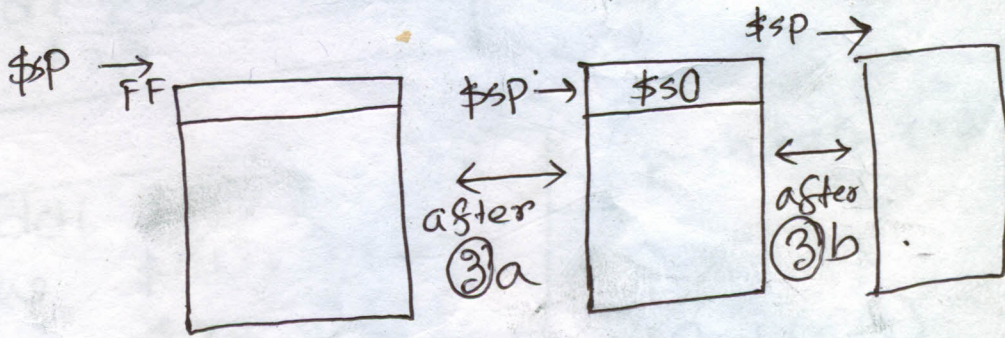
```
int test(int g, h, i, j) {
    int s = (g+h) - (i+j);
    return s;
}
```

3

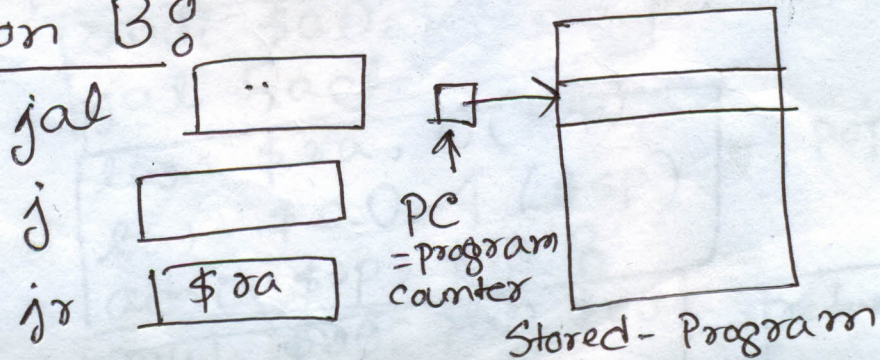
$g \leftrightarrow \$a0$	$s \leftrightarrow \$s0$
\vdots	$g+h \leftrightarrow \$t0$
$j \leftrightarrow \$a3$	$i+j \leftrightarrow \$t1$

↗ push to stack

```
test:
3a addi $sp, $sp, -4
   sw $s0, 0($sp)
4  add $t0, $a0, $a1
   add $t1, $a2, $a3
   sub $s0, $t0, $t1
5  add $v0, $s0, $zero
3b lw $s0, 0($sp)
   addi $sp, $sp, 4
6  jr $ra
```



For Section B:



ated Procedure :

main

100: A (3) \rightarrow A

$\$ra = 104$
 $\$a0 = 3$

200: B (7) \rightarrow B

$\$ra = 204$
 $\$a0 = 7$

so we must save

$\$ra$ (1) & $\$a0$ (2)

C

$1 \ n \leftrightarrow \$a0$

0

①

②

```

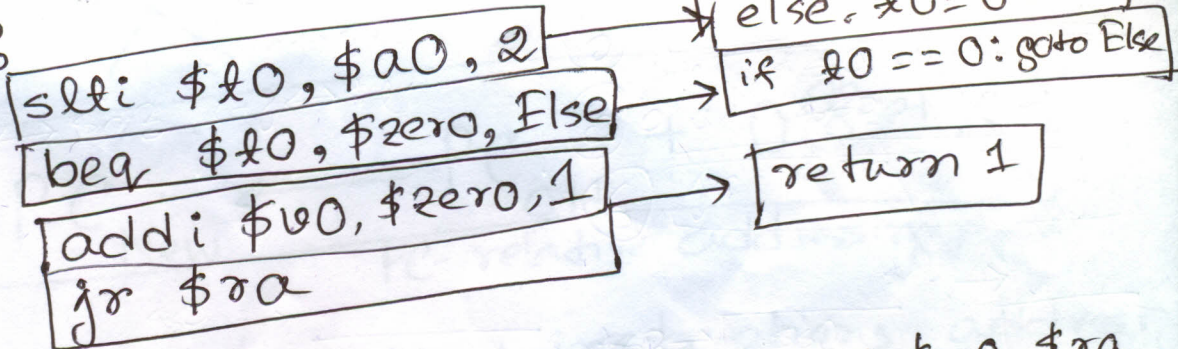
int fact(int n) {
  if (n < 2) return 1;
  else return n * fact(n-1);
}

```

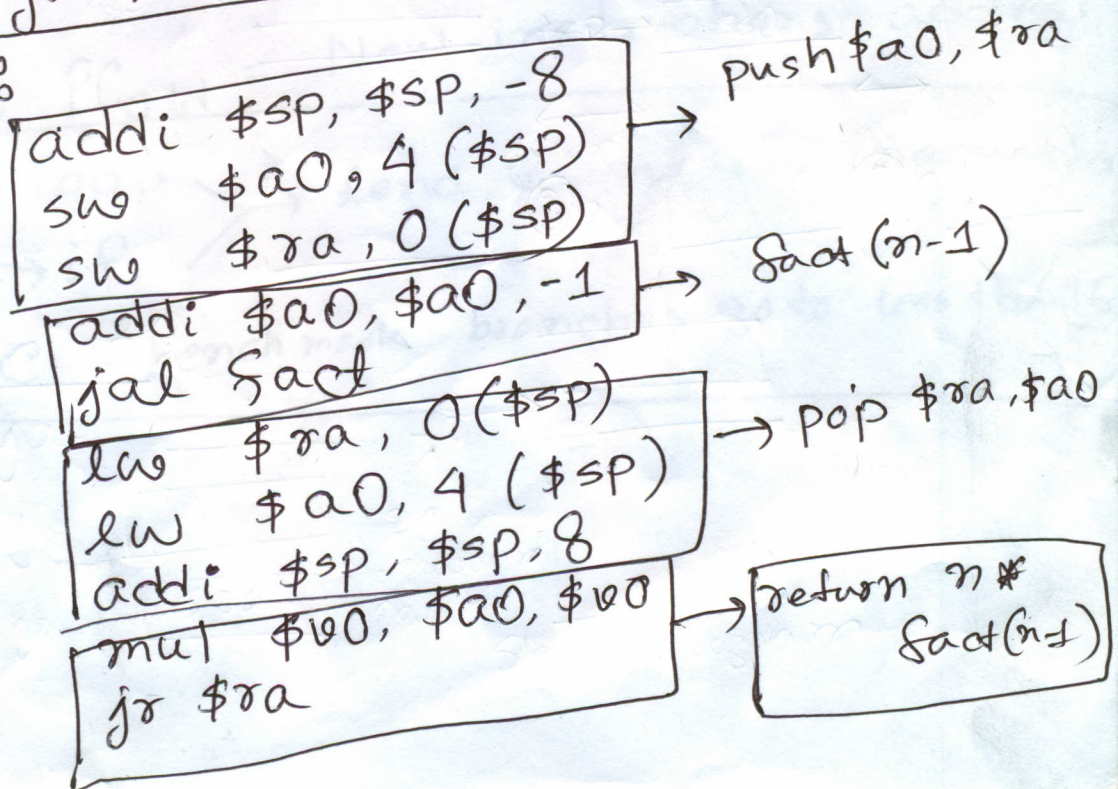
$n \leftrightarrow \$a0$

return result
 \updownarrow
 $\$v0$

fact :



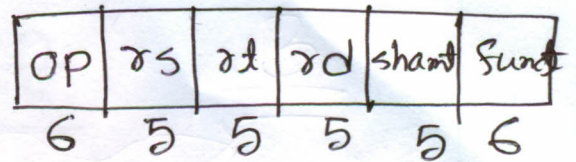
Else :



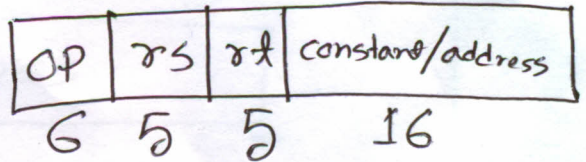
coding Branch Instructions in 32-bit binary

Recap:

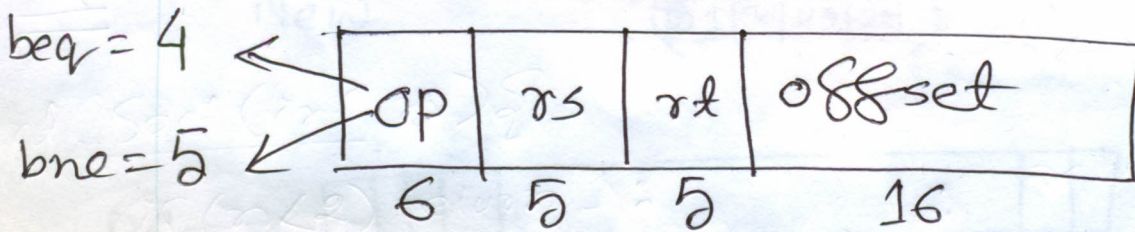
R-format



I-format



→ branch → beq \$r1, \$r2, label
 → bne \$r1, \$r2, label



offset address 16-bit,

~~only, 65536 - instructions~~

$$PC_{New} \leftarrow PC_{old} + offset \times 4$$

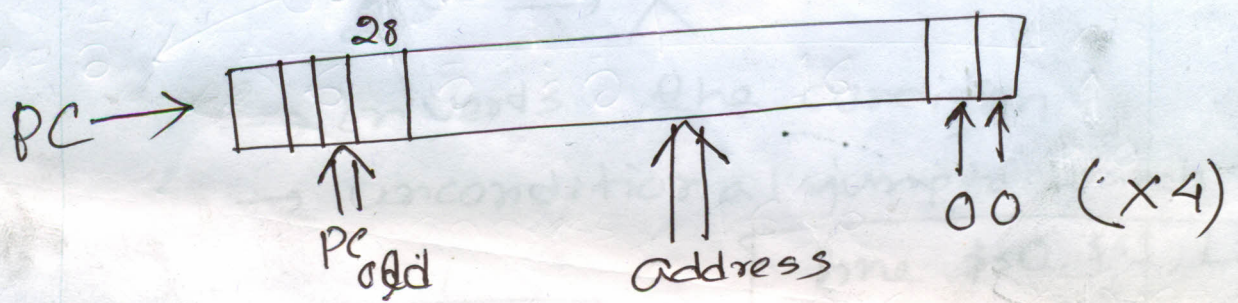
PC-relative addressing

~ PC_{old} = Next instructions address

branch → loop → tend to nearby instructions
 → if

$\frac{1}{2}$ SPEC bench mark branches go to less than 16

$$PC_{New} = PC_{Old}(\boxed{31} \boxed{30} \boxed{29} \boxed{28}) : (\text{address} \times 4)$$



Example:

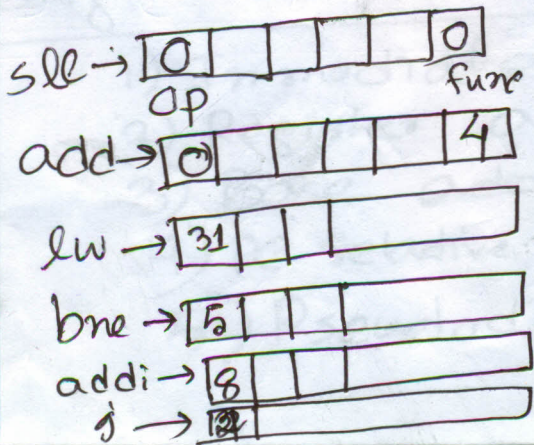
```
while (save[i] == k) i++;
```

i ← \$s3
k ← \$s5
save ← \$s6

```
loop: sll $t1, $s3, 2
      add $t1, $t1, $s6
      lw $t0, 0($t1)
      bne $t0, $s5, Exit
      addi $s3, $s3, 1
      j Loop
```

$t1 \leftarrow t1 * 4$
 $t1 \leftarrow \text{save} + (t1 * 4)$

Exit:



- 4000 : ~~sll \$t1, \$s3, 2~~
- 4004 : ~~add \$t1, \$t1, \$s6~~
- 4008 :
- 4012 :
- 4016 :
- 4020 :
- 4024 :

	opcode	rs	rt	rd	shamt	function
	6	5	5	5	5	6
400%	0	0	19	9	2	0
404%	0	9	22	9	0	4
408%	31	9	8		0	
412%	5	8	21		2	
416%	8	19	19		1	
420%	2					400
424%						

* Branching far away:

$$2^{16} \rightarrow X$$

→ inverts the condition

→ unconditional jump to branch ~~address~~

beq \$s0, \$s1, L1



bne \$s0, \$s1, L2
j L1
L2:

MIPS instruction format summary:

	opcode					
	6	5	5	5	5	6
R	OP	rs	rt	rd	shamt	func
I	OP	rs	rt	address/immediate		
J	OP	target Address				
	6	5	5	5	5	6

Addressing Mode Summary:

- 1) Immediate addressing
- 2) Register addressing
- 3) Base addressing
- 4) PC-relative addressing
- 5) Pseudodirect addressing

BT Decoding Machine Code:

Why? — 'core dump'

0x15320001 → bne \$t1, \$s2, 52

0x0800000A → j 40

0x01135004 → add \$t2, \$t0, \$s3

00010101001100100000-----1
 00010-----1010
 00000100001001101010000000100

40:

44:	5	9	18	1	bne \$t1, \$s2, 52		
48:	2	10			j 40		
52:	0	8	19	10	0	4	add \$t2, \$t0, \$s3
	6	5	5	5	5	6	

0000 0001 0001 0011 0101 0000 0000
 0 1 1 3 5 0 0100
 4