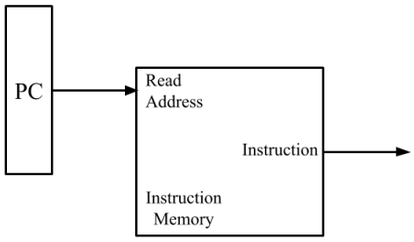
Bangladesh University of Engineering & Technology (BUET)
Dept. of Computer Science & Engineering (CSE)

CSE 305: Computer Architecture
Class Test 3, July 2015

Time: 20 minutes Full Marks: 20

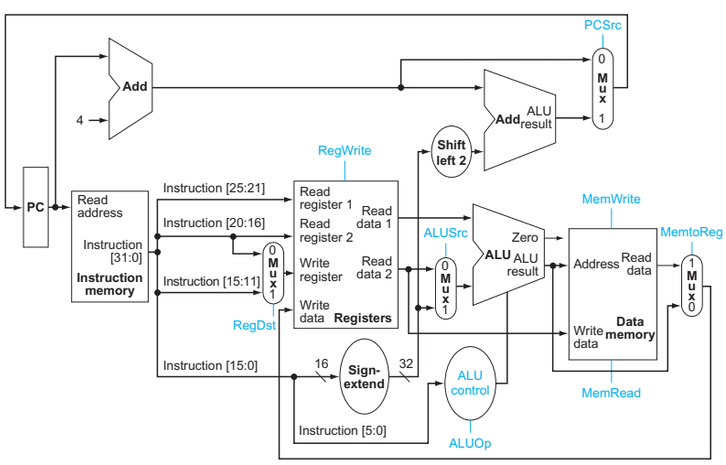
Name:	Student No.:

1. The basic instruction fetch unit of MIPS computer system is given below. Please add the necessary elements to it so that it can incorporate-
   - general sequential execution 2
   - "`beq`" instruction execution 2
   - "`j`" instruction execution 3



2. A simple MIPS datapath and its respective control signals are illustrated below. Please design the control bits corresponding to the instruction "`sw rt, 0(rs)`" for this datapath. $6 \times \frac{1}{2} = 3$

Control Signal	0	1	**SW**
RegDst	Write register address = `rt`	Write register address = `rd`	
RegWrite	-	Write register	
ALUSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction	
MemRead	-	Read data from memory	
MemWrite	-	Write data into memory	
MemtoReg	Register Write Data from ALU	Register Write Data from data memory	



3. What problem will the computer industry face if they continue to increase the clock frequency to make the computers faster? 3

4. What is the required property of a data path for pipeline implementation? 2

5. What do you mean by structural hazard in instruction pipelining? How is it overcome? Explain with time-space diagram. 5