CSE 305: Computer Architecture

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Recap

CPU Clock Cycles

- computers are constructed using a clock that determines when events take place
- these discrete time intervals are called clock cycles, or clock cycle time
- clock period, the time for a complete clock cycle

$$\text{clock rate} = \frac{1}{\text{clock period}}$$

$$\begin{array}{c}\text{CPU execution time}\\ \text{for a program}\end{array} = \begin{array}{c}\text{CPU clock cycles}\\ \text{for a program}\end{array} \times \text{Clock cycle time}$$

$$\begin{array}{c}\text{CPU execution time}\\ \text{for a program}\end{array} = \frac{\text{CPU clock cycles for a program}}{\text{Clock rate}}$$

Instruction Performance

- execution time for a program depends on number of instructions in a program
- average number of clock cycles per instruction is abbreviated as CPI
- number of clock cycles required for a program can be written as,

$$\text{CPU clock cycles} = \text{Instructions for a program} \times \begin{array}{c}\text{Average clock cycles}\\ \text{per instruction}\end{array}$$

The Classic CPU Performance Equation

$$\text{CPU time} = \text{Instruction count} \times \text{CPI} \times \text{Clock cycle time}$$

$$\text{CPU time} = \frac{\text{Instruction count} \times \text{CPI}}{\text{Clock rate}}$$

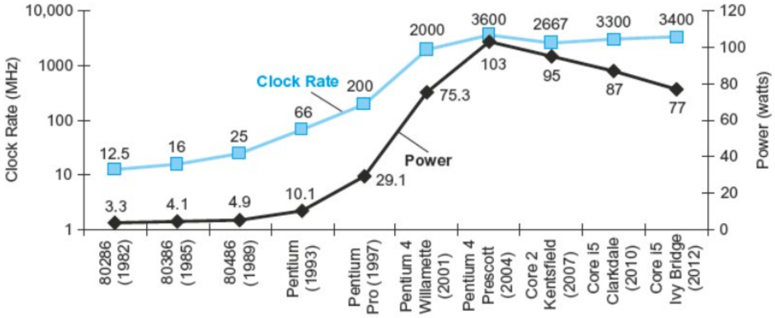
$$\text{Time} = \frac{\text{Seconds}}{\text{Program}} = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Clock cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Clock cycle}}$$

Today's Topic

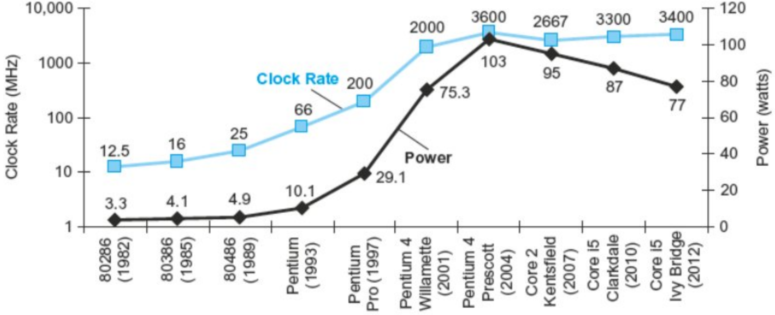
Outline

- The power wall
- The switch from uniprocessors to multiprocessors
- Benchmarking the intel core i7
- Fallacies and Pitfalls

The Power Wall



The Power Wall



Power and clock rate are correlated.

The Power Wall

Correlation Between Power & Clock Rate

- dynamic energy equation of pulse during the CMOS logic transition of $0 \to 1 \to 0$,

$$\text{Energy} \propto \text{Capacitive load} \times \text{Voltage}^2$$

The Power Wall

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- The power required per transistor is just the product of energy of a transition and the frequency of transitions:

$$\text{Energy} \propto \frac{1}{2} \times \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency switched}$$

The Power Wall

Example

Suppose we developed a new, simpler processor that has 85% of the capacitive load of the more complex older processor. Further, assume that it has adjustable voltage so that it can reduce voltage 15% compared to processor B, which results in a 15% shrink in frequency. What is the impact on dynamic power?

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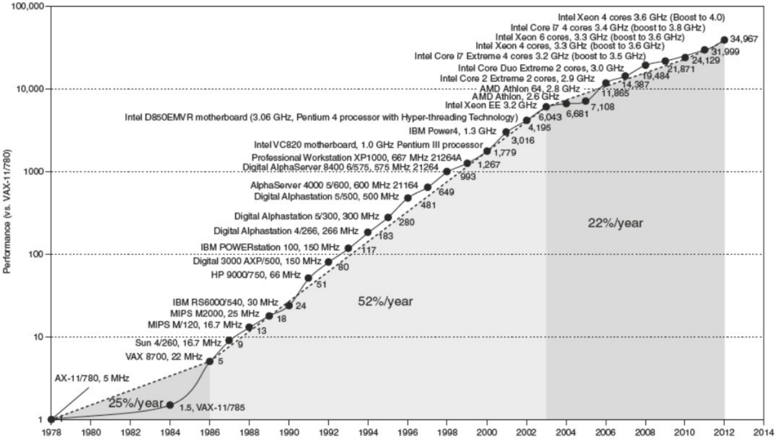
The Switch from Uniprocessors to Multiprocessors



Benchmarking The Intel Core i7

Description	Name	Instruction Count x 10^9	CPI	Clock cycle time (seconds x 10^{-9})	Execution Time (seconds)	Reference Time (seconds)	SPECratio
Interpreted string processing	perl	2252	0.60	0.376	508	9770	19.2
Block-sorting compression	bzip2	2390	0.70	0.376	629	9650	15.4
GNU C compiler	gcc	794	1.20	0.376	358	8050	22.5
Combinatorial optimization	mcf	221	2.66	0.376	221	9120	41.2
Go game (AI)	go	1274	1.10	0.376	527	10490	19.9
Search gene sequence	hmmer	2616	0.60	0.376	590	9330	15.8
Chess game (AI)	sjeng	1948	0.80	0.376	586	12100	20.7
Quantum computer simulation	libquantum	659	0.44	0.376	109	20720	190.0
Video compression	h264avc	3793	0.50	0.376	713	22130	31.0
Discrete event simulation library	omnetpp	367	2.10	0.376	290	6250	21.5
Games/path finding	astar	1250	1.00	0.376	470	7020	14.9
XML parsing	xalancbmk	1045	0.70	0.376	275	6900	25.1
Geometric mean	–	–	–	–	–	–	25.7

Suppose a program runs in 100 seconds on a computer, with multiply operations responsible for 80 seconds of this time. How much do I have to improve the speed of multiplication if I want my program to run five times faster?

Fallacies and Pitfalls

Amdahl's Law

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$$\text{Execution time after improvement} =$$
$$\frac{\text{Execution time affected by improvement}}{\text{Amount of improvement}} + \text{Execution time unaffectted}$$

- Computers at low utilization use little power.
- Designing for performance and designing for energy efficiency are unrelated goals.

Fallacies and Pitfalls

Pitfall

- Using a subset of the performance equation as a performance metric.

MIPS, (million instructions per second),

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$$\text{MIPS} = \frac{\text{Clock rate}}{\text{CPI} \times 10^6}$$

Fallacies and Pitfalls

Example

Consider the following performance measurements for a program:

Measurement	Computer A	Computer B
Instruction count	10 billion	8 billion
Clock rate	4 GHz	4 GHz
CPI	1.0	1.1

a. Which computer has the higher MIPS rating?

b. Which computer is faster?

Reference

- Computer Organization and Design: The Hardware/Software Interface, *Chapter 1, 1.7-1.10*
  - David A. Patterson
  - John L. Hennessy