CSE 305: Computer Architecture

Tanvir Ahmed Khan

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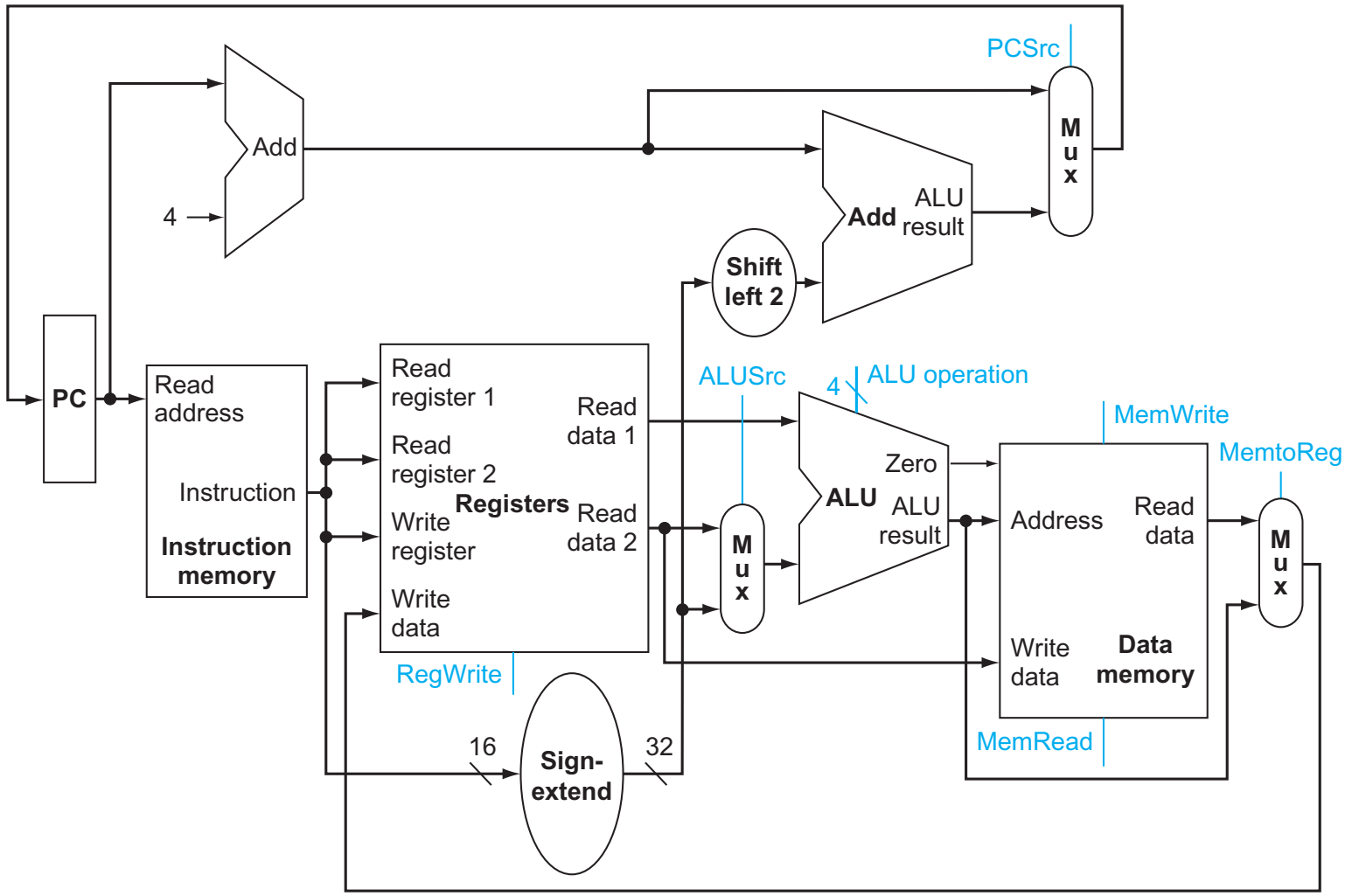
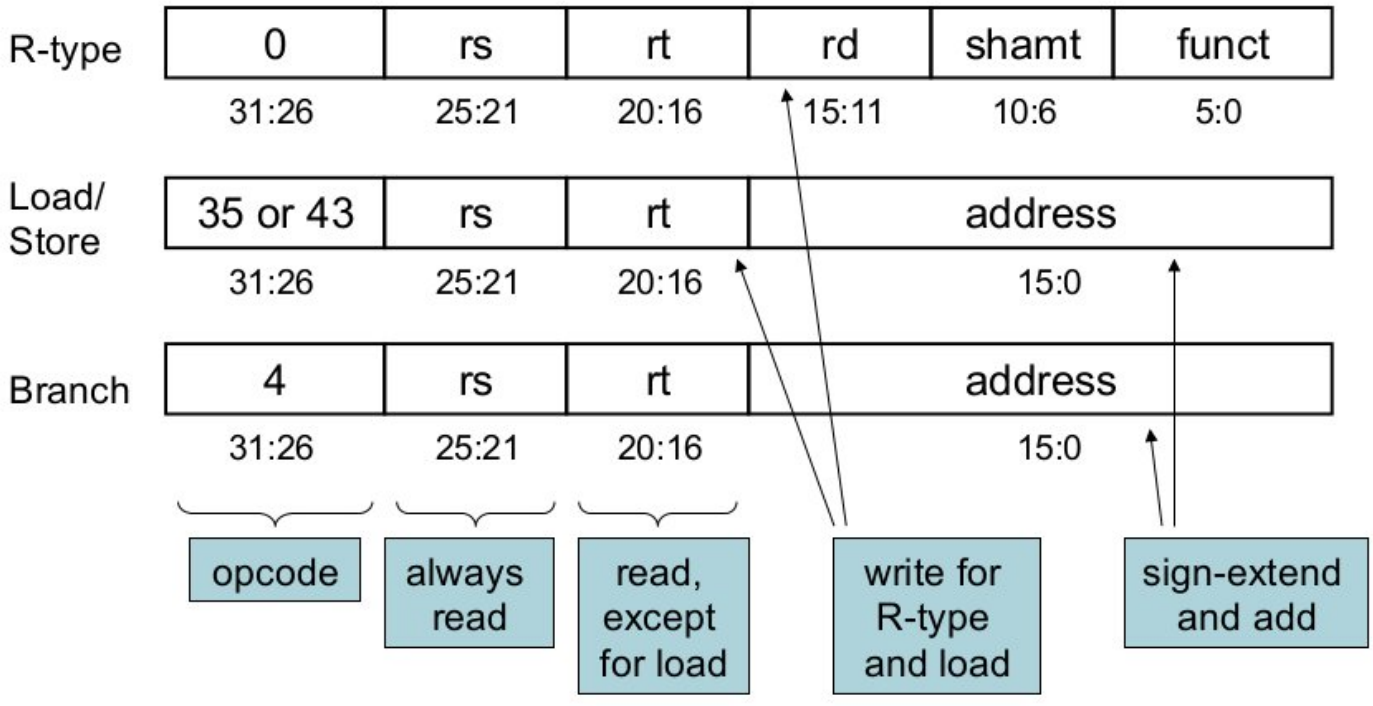
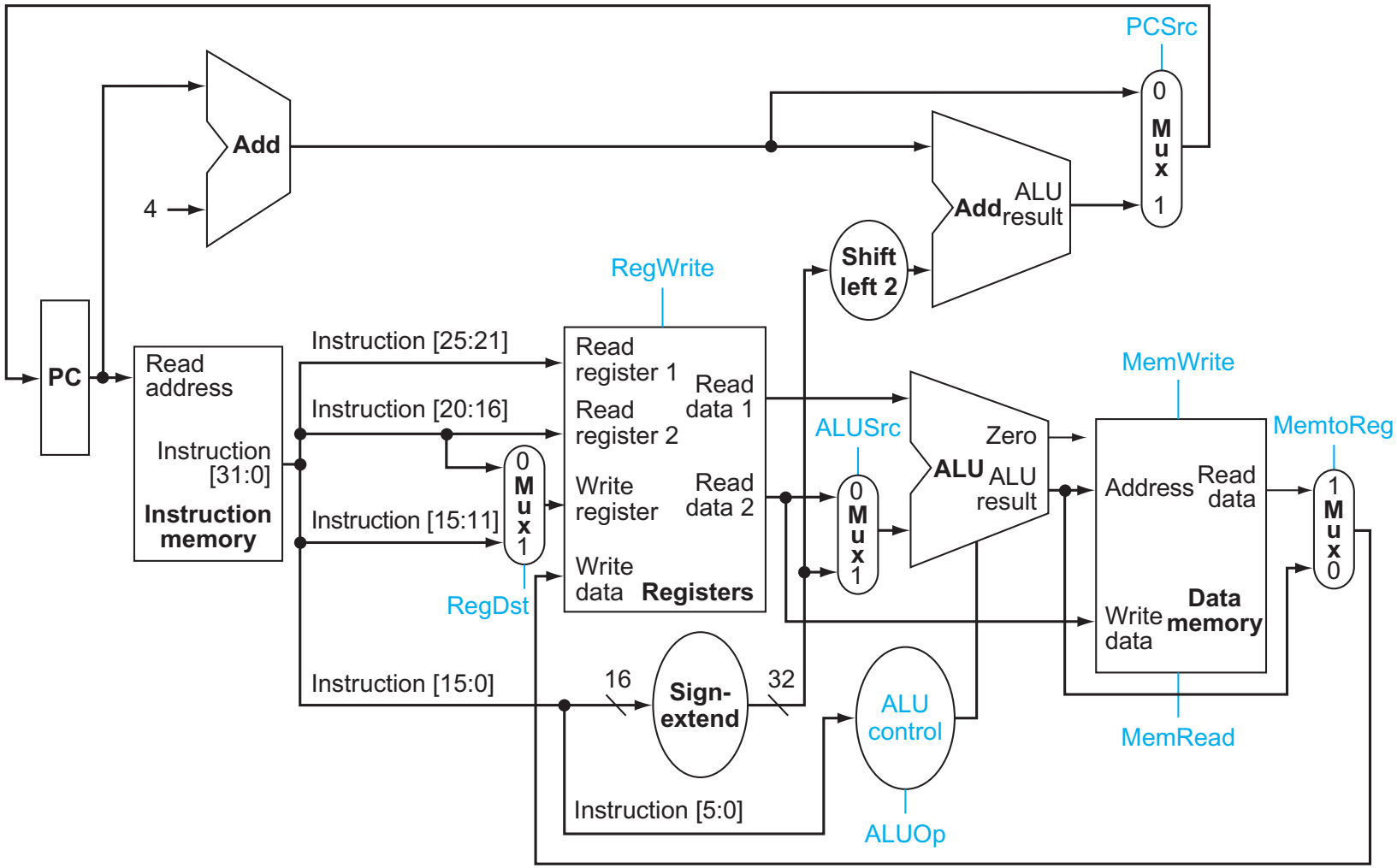
Department of Computer Science and Engineering
Bangladesh University of Engineering and Technology.

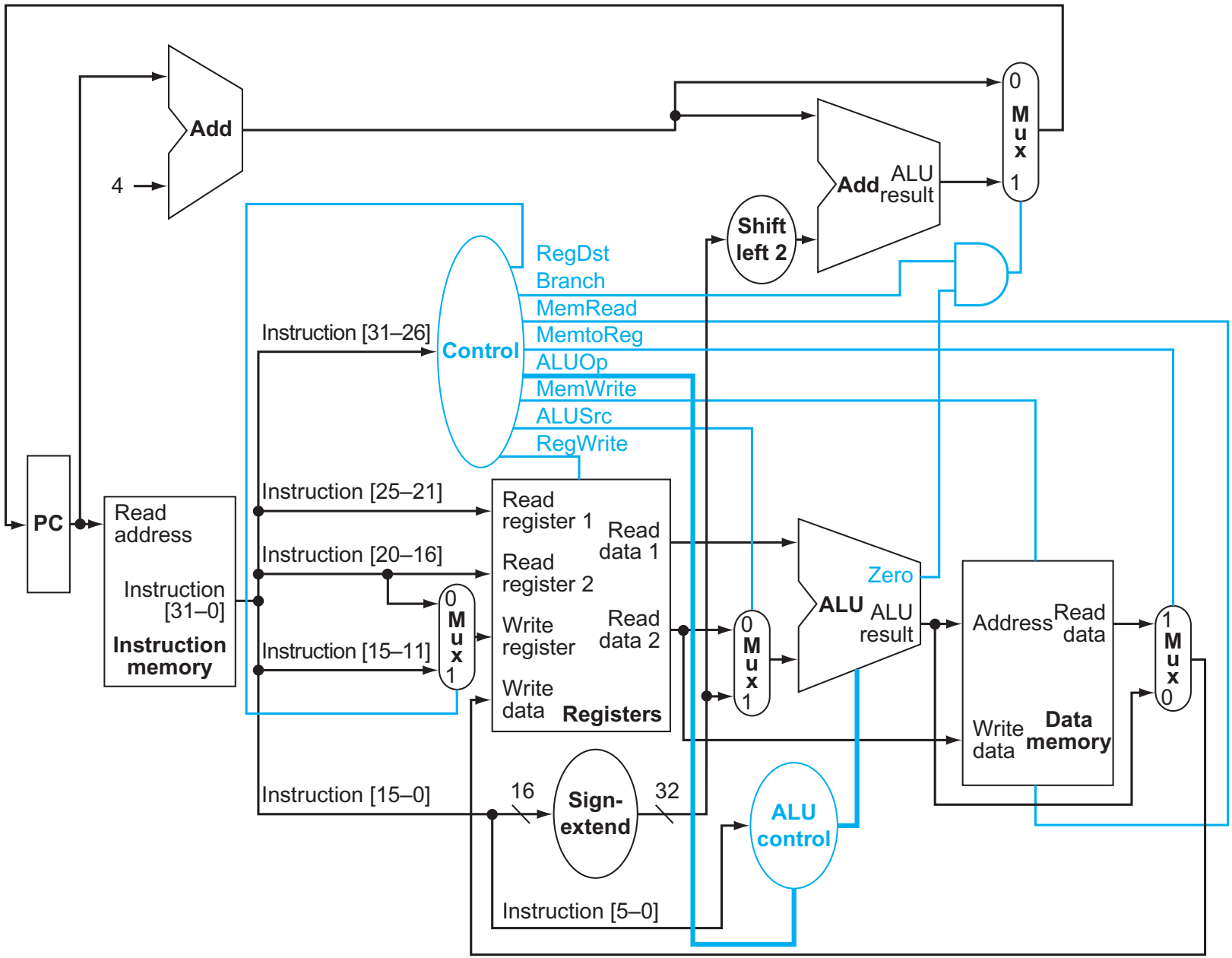
November 8, 2015

Recap


PCSrc
Add
4
M
u
x
Add
ALU
result
Shift
left 2
PC
Read
address
Instruction
Instruction
memory
Read
register 1
Read
register 2
Registers
Write
register
Write
data
Read
data 1
Read
data 2
RegWrite
ALUSrc
4
ALU operation
M
u
x
ALU
Zero
ALU
result
MemWrite
MemtoReg
Address
Read
data
Write
data
Data
memory
MemRead
M
u
x
16
Sign-
extend
32


R-type
0
rs
rt
rd
shamt
funct
31:26
25:21
20:16
15:11
10:6
5:0
Load/
Store
35 or 43
rs
rt
address
31:26
25:21
20:16
15:0
Branch
4
rs
rt
address
31:26
25:21
20:16
15:0
opcode
always
read
read,
except
for load
write for
R-type
and load
sign-extend
and add


PCSrc
Add
4
0
M
u
x
1
Add
ALU result
Shift left 2
RegWrite
PC
Read address
Instruction [31:0]
Instruction memory
Instruction [25:21]
Instruction [20:16]
Instruction [15:11]
Instruction [15:0]
Instruction [5:0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
RegDst
ALUSrc
Zero
ALU
ALU result
MemWrite
MemtoReg
Address
Read data
Write data
Data memory
MemRead
16
Sign-extend
32
ALU control
ALUOp


Add
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Shift
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MemtoReg
ALUOp
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0

Today's Topic

Control Unit

Control Signal Summary

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
PCSrc	PC=PC+4	PC=branch target
MemRead	-	Read data from memory
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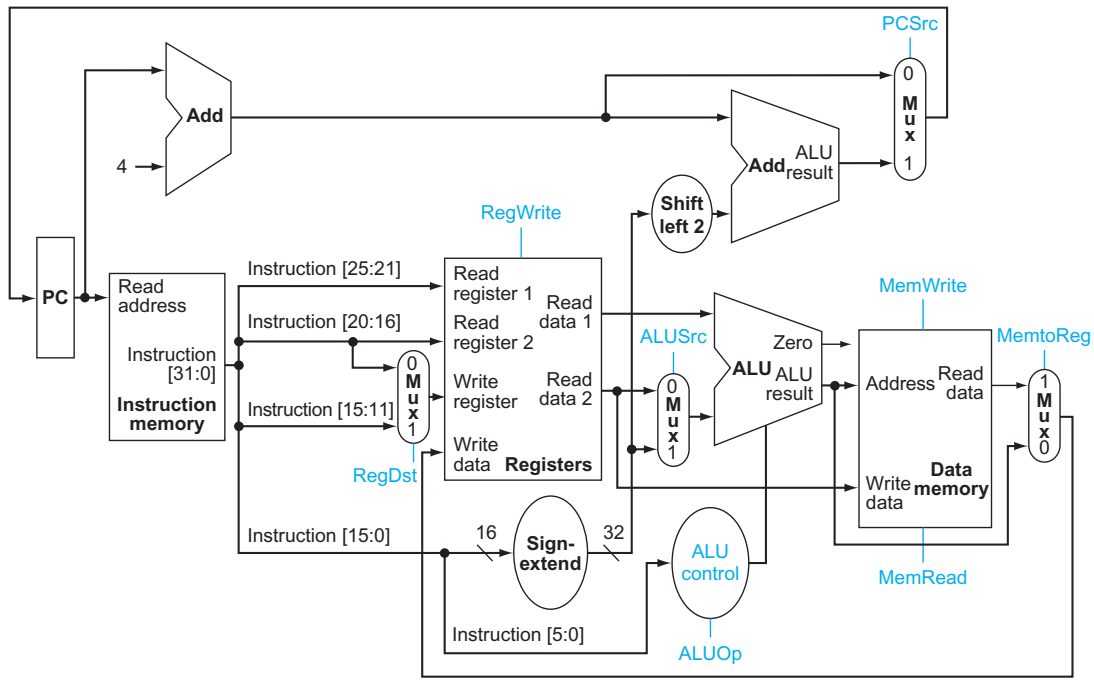
MemtoReg	Register Write Data from ALU	Register Write Data from data memory



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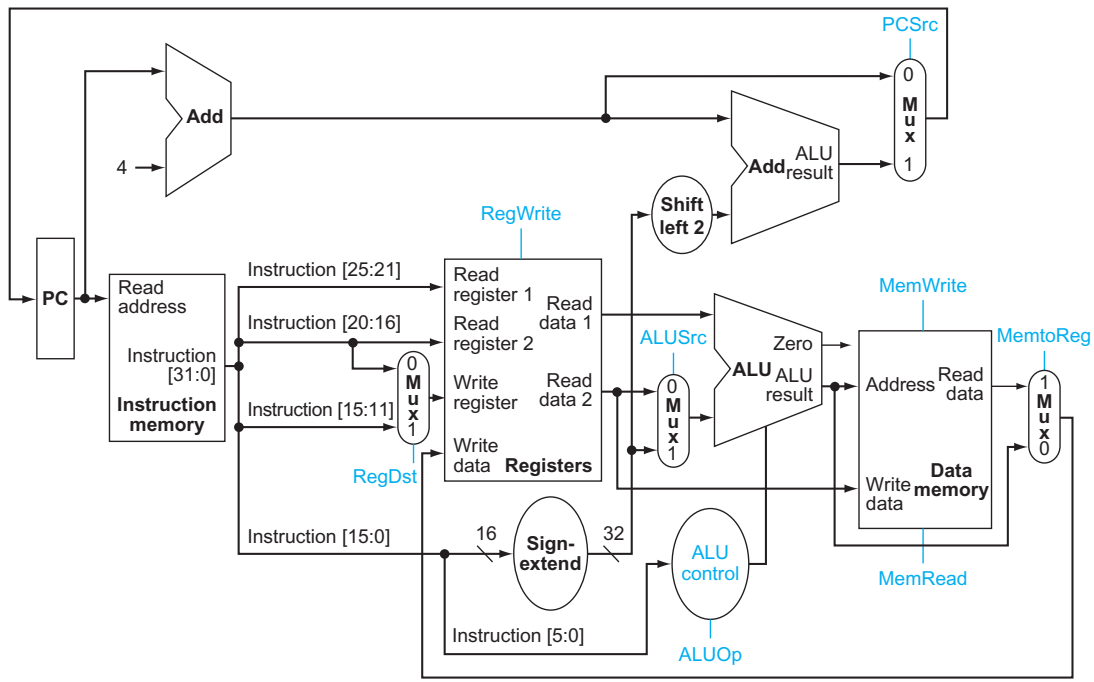

lw rt, 0(rs)

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lw							

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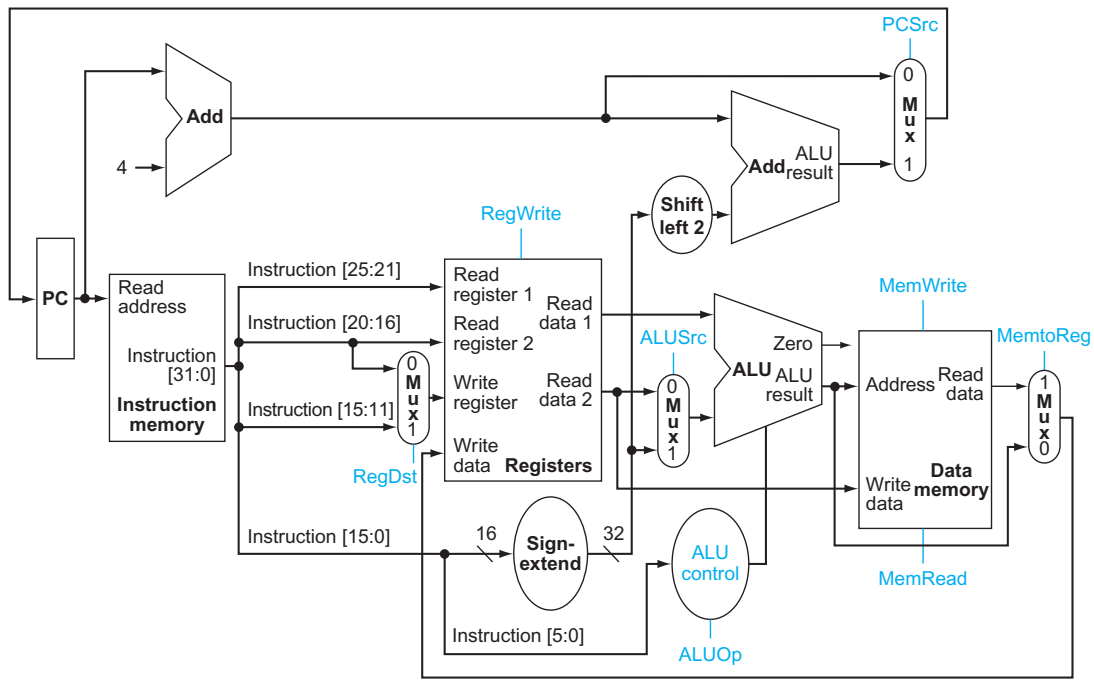

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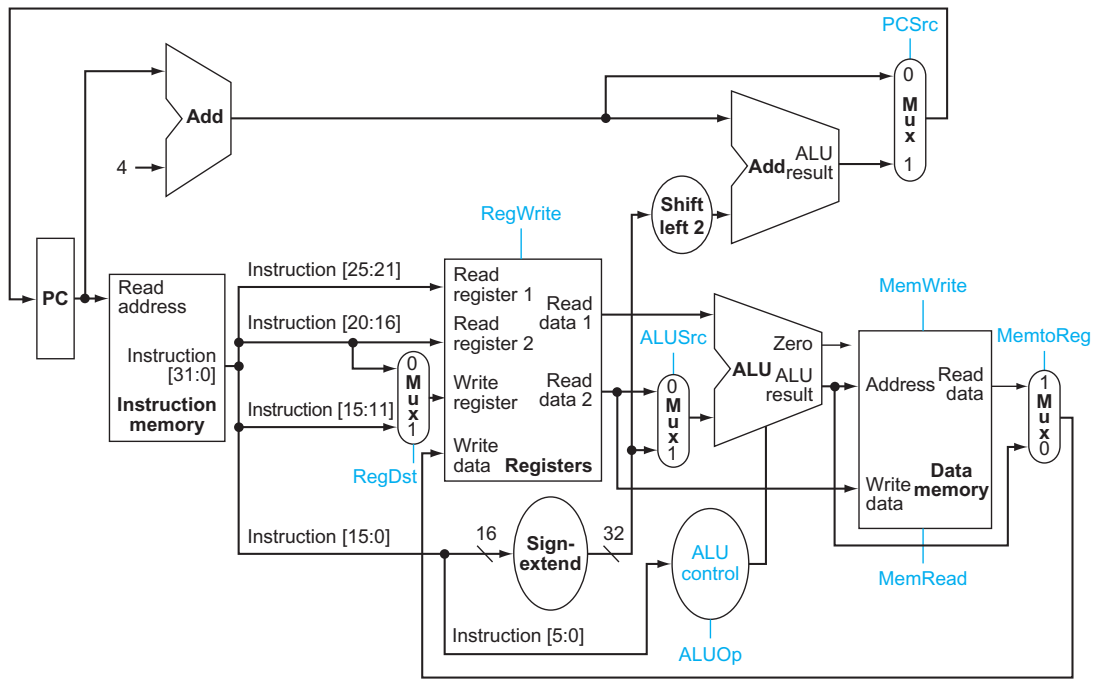

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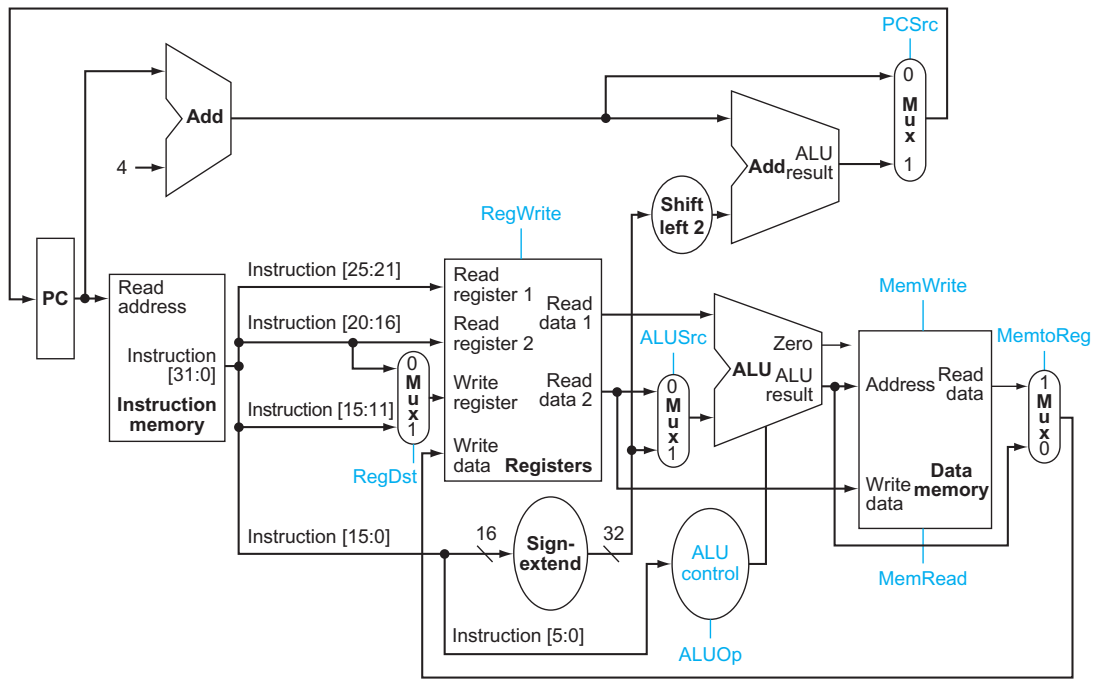

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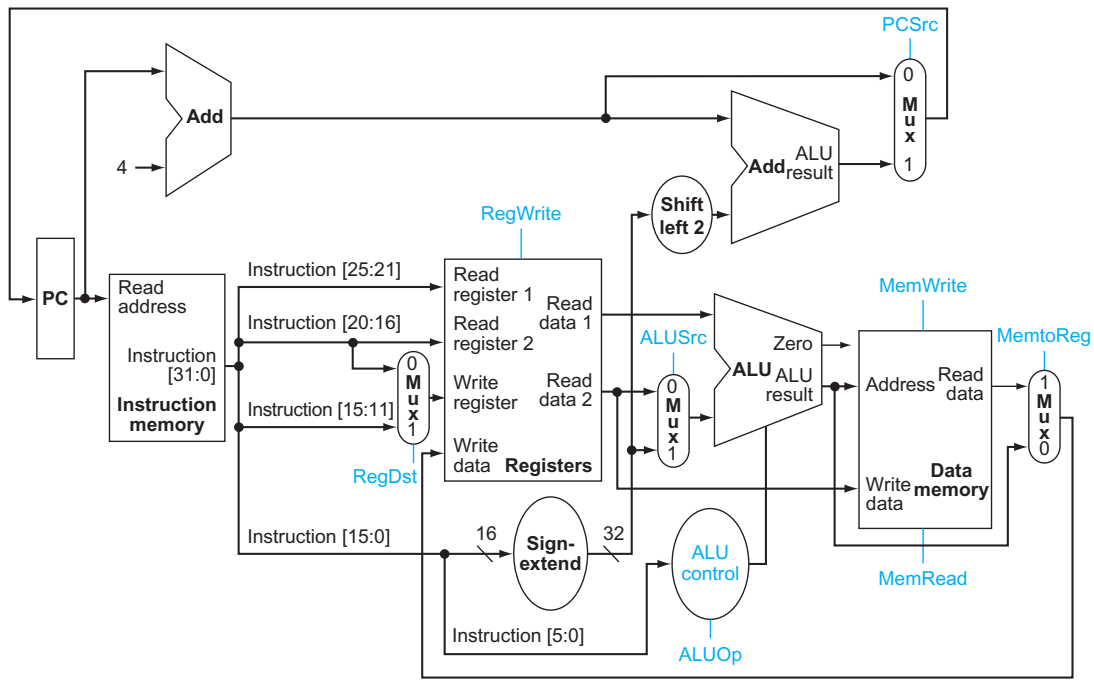

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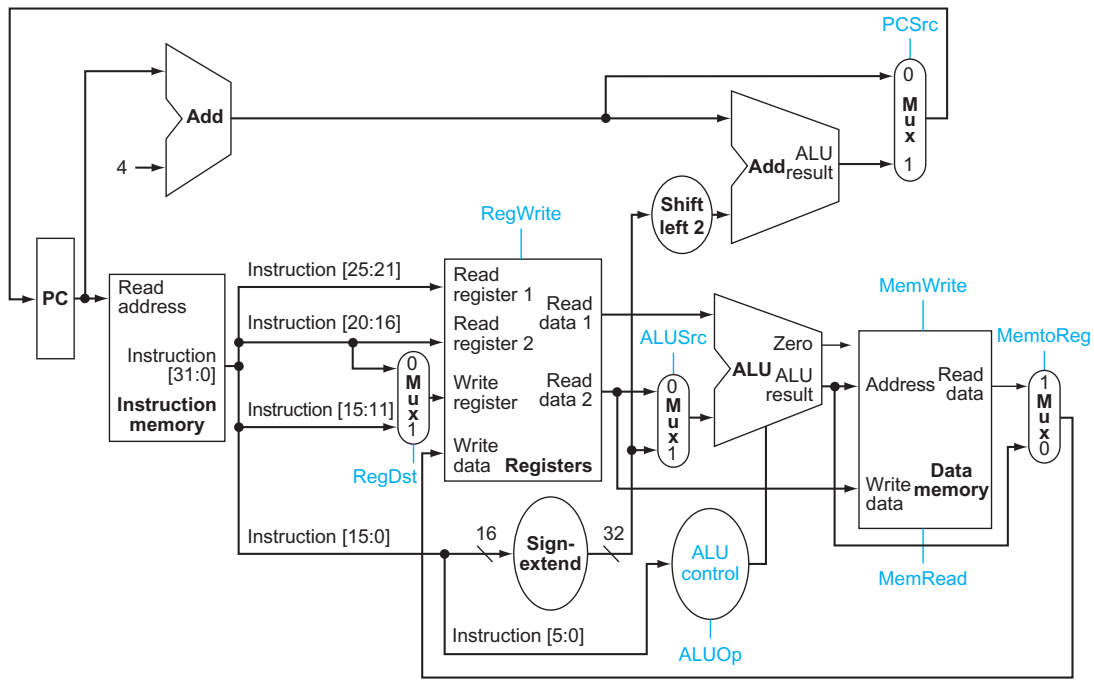

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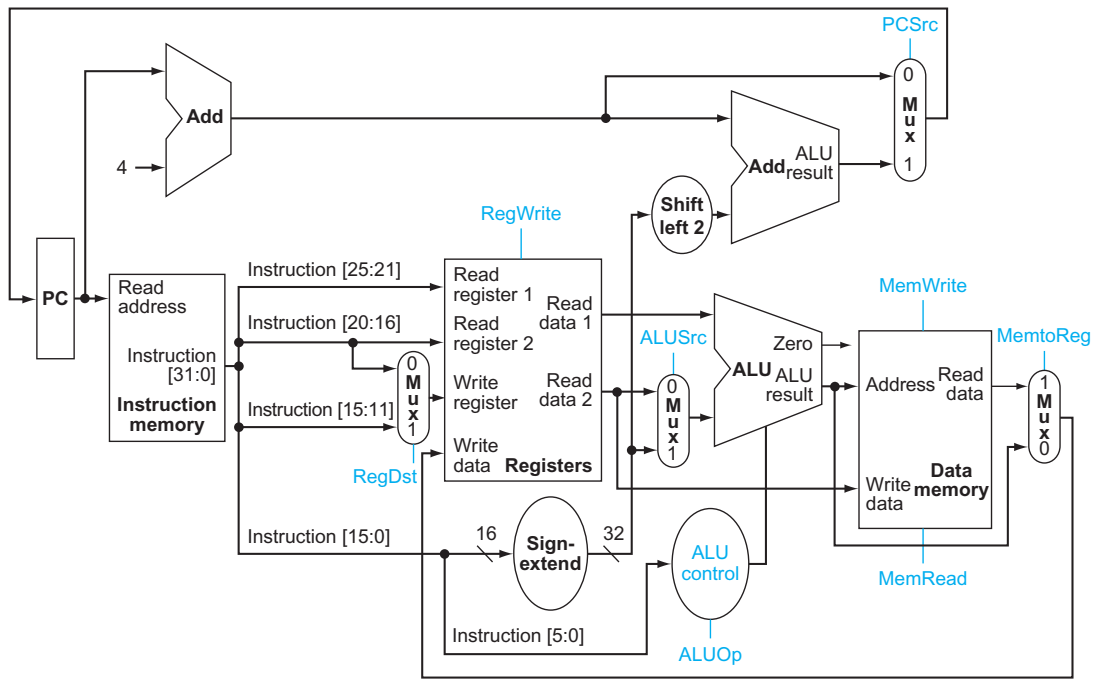

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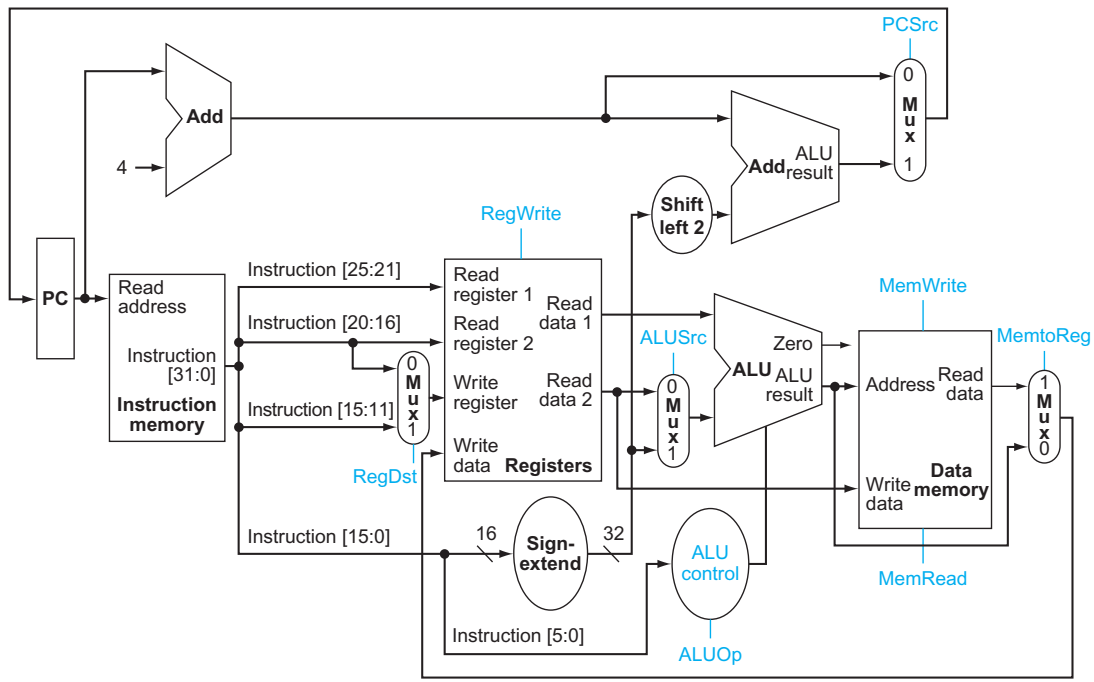

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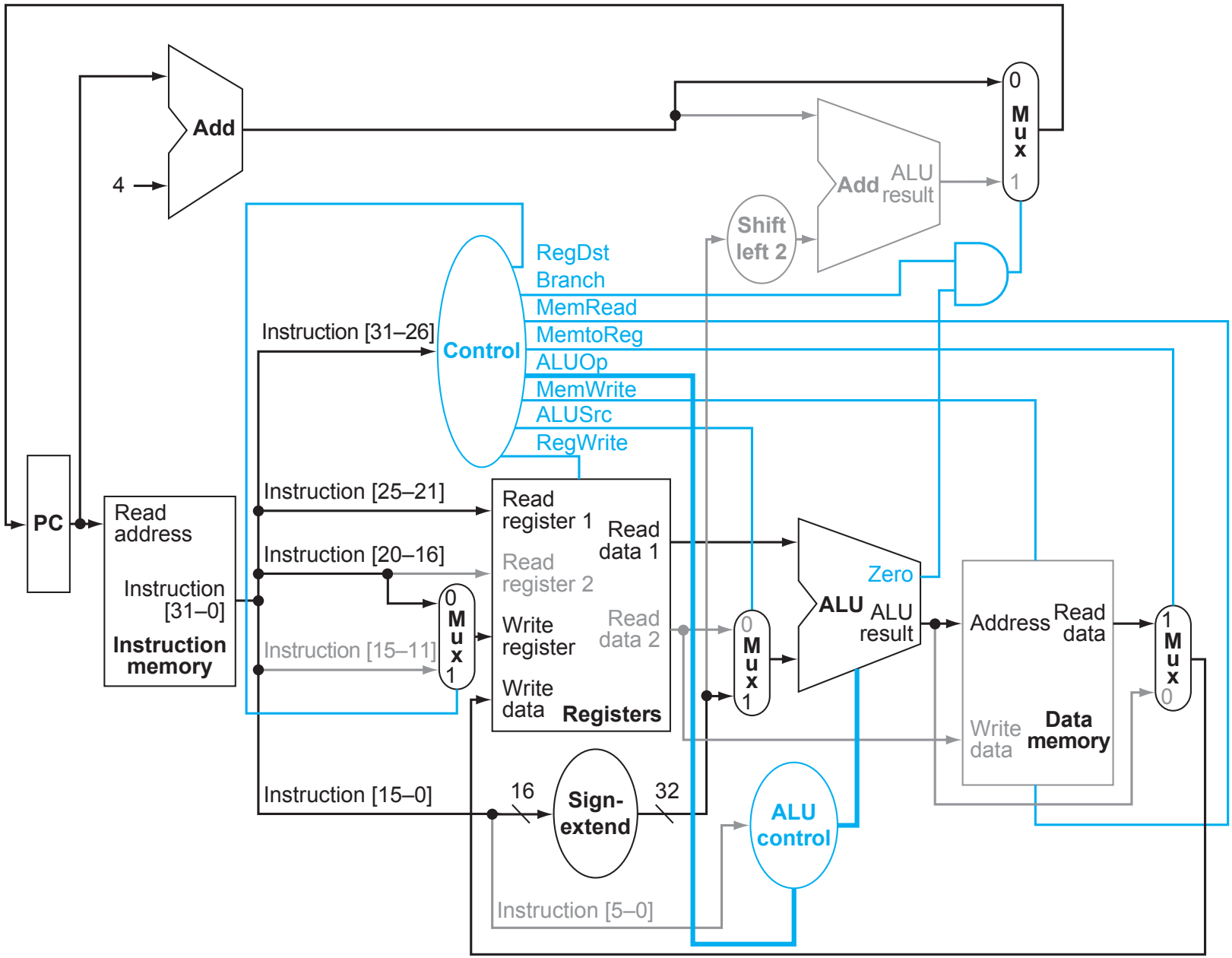
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Shift left 2
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ALU control

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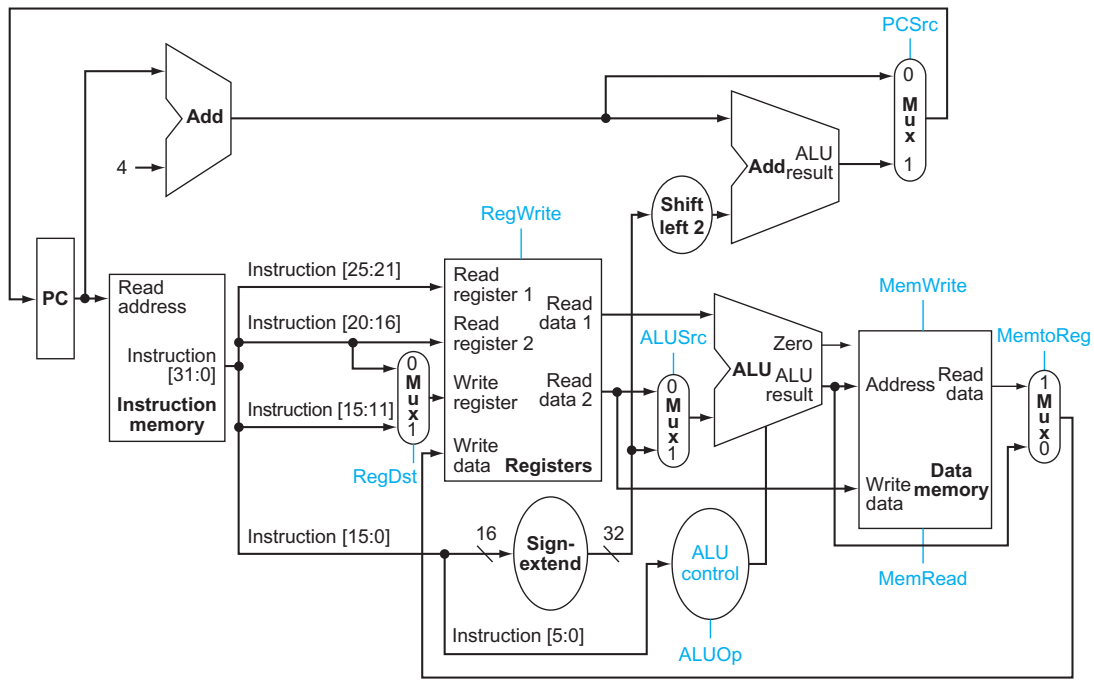

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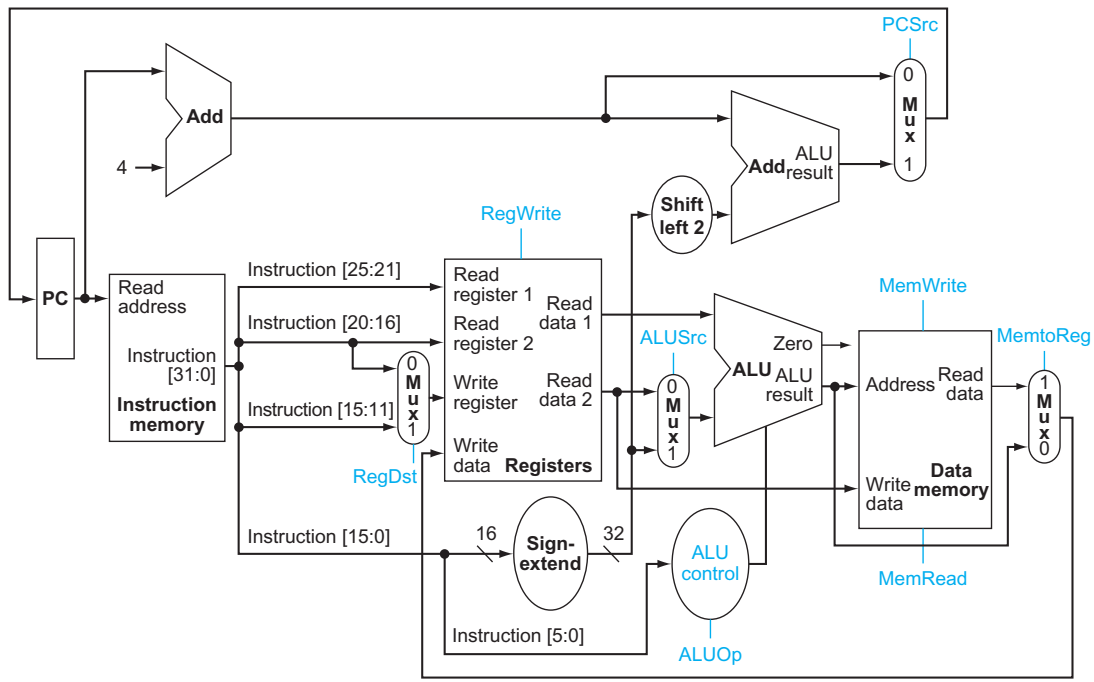

sw rt, 0(rs)

	RegDst	**RegWrite**	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
sw	X						

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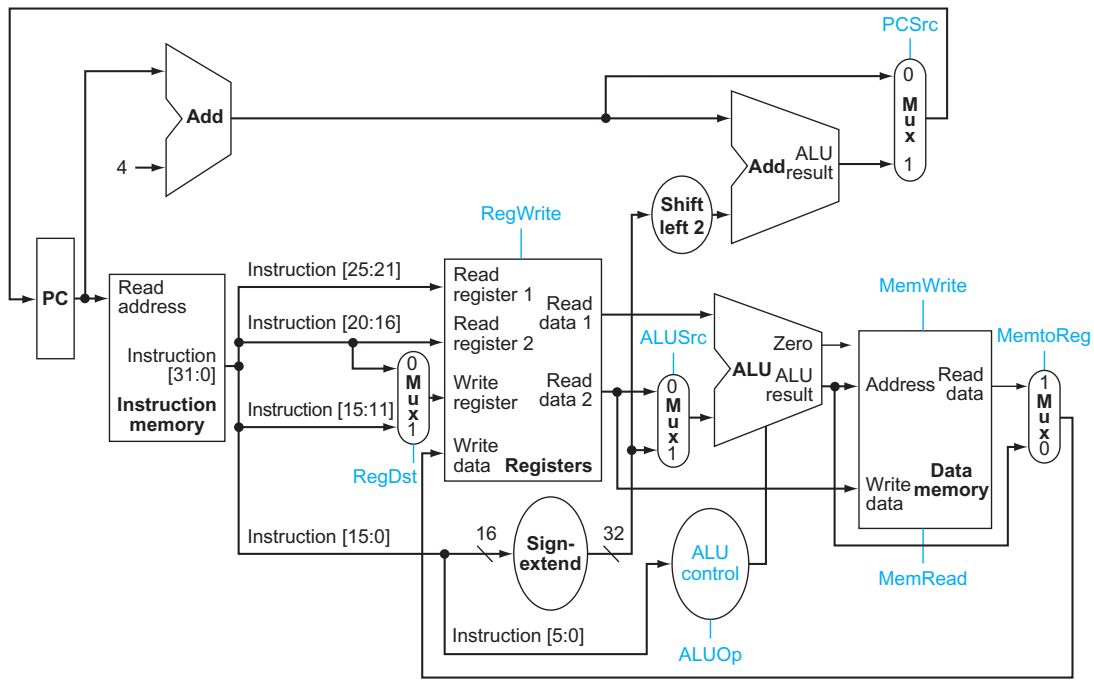

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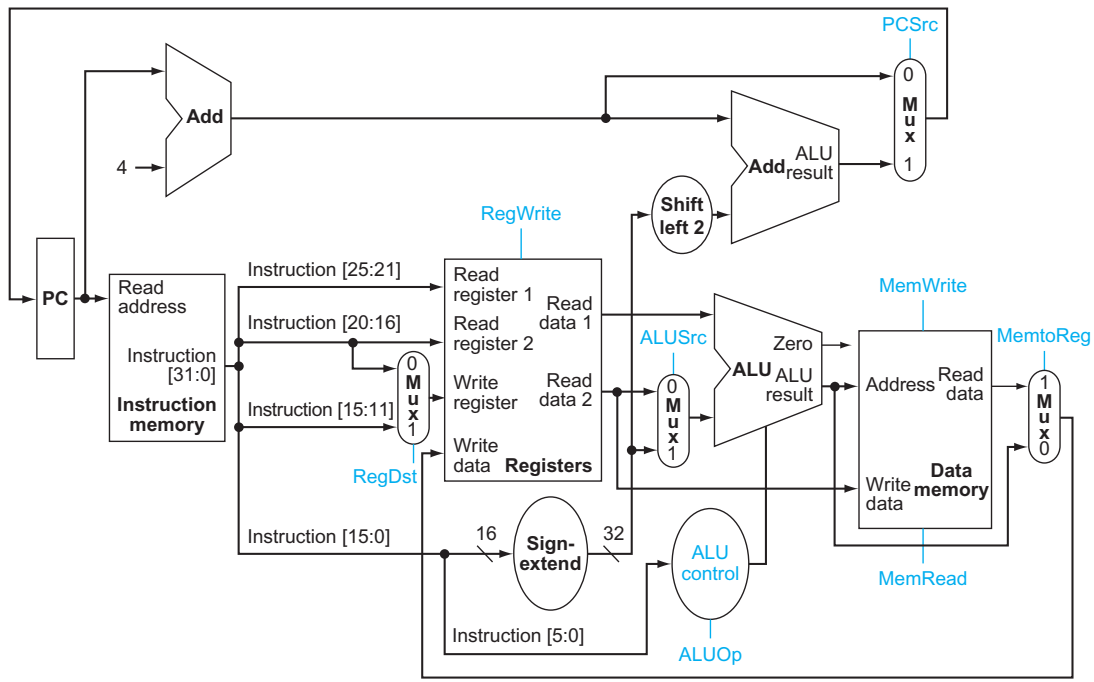

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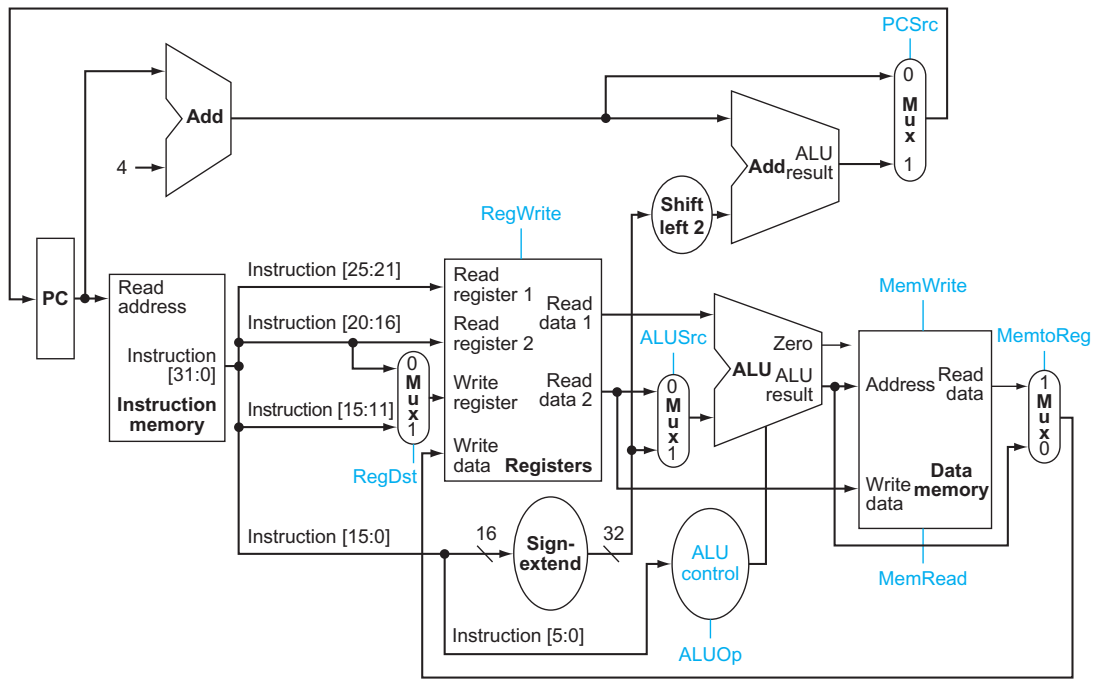

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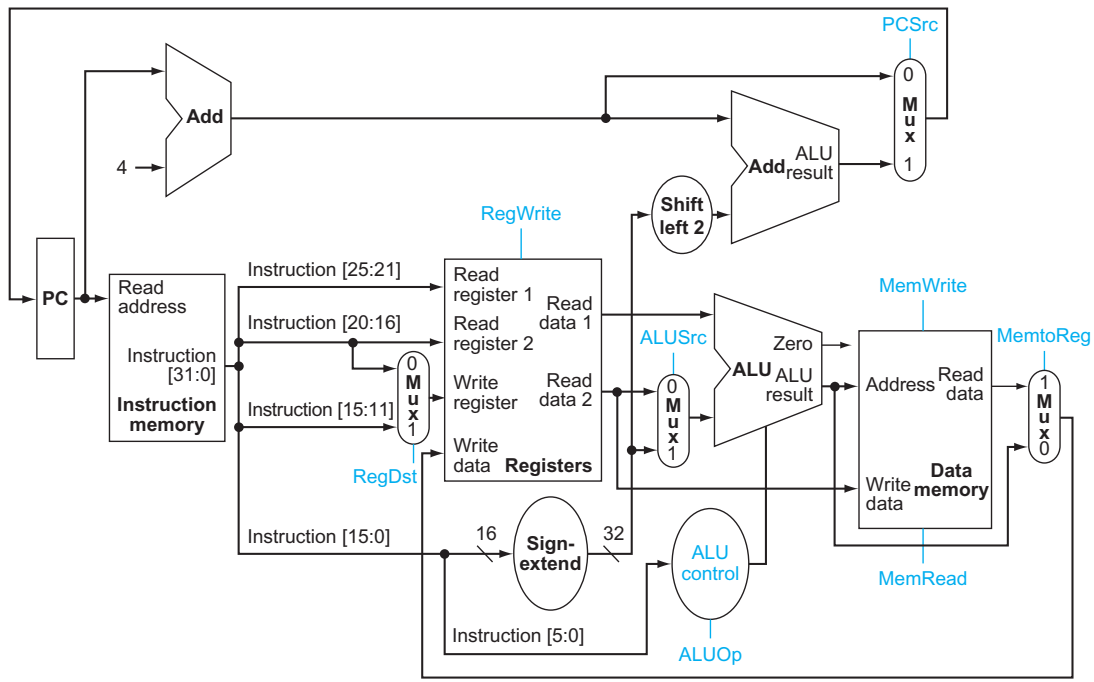

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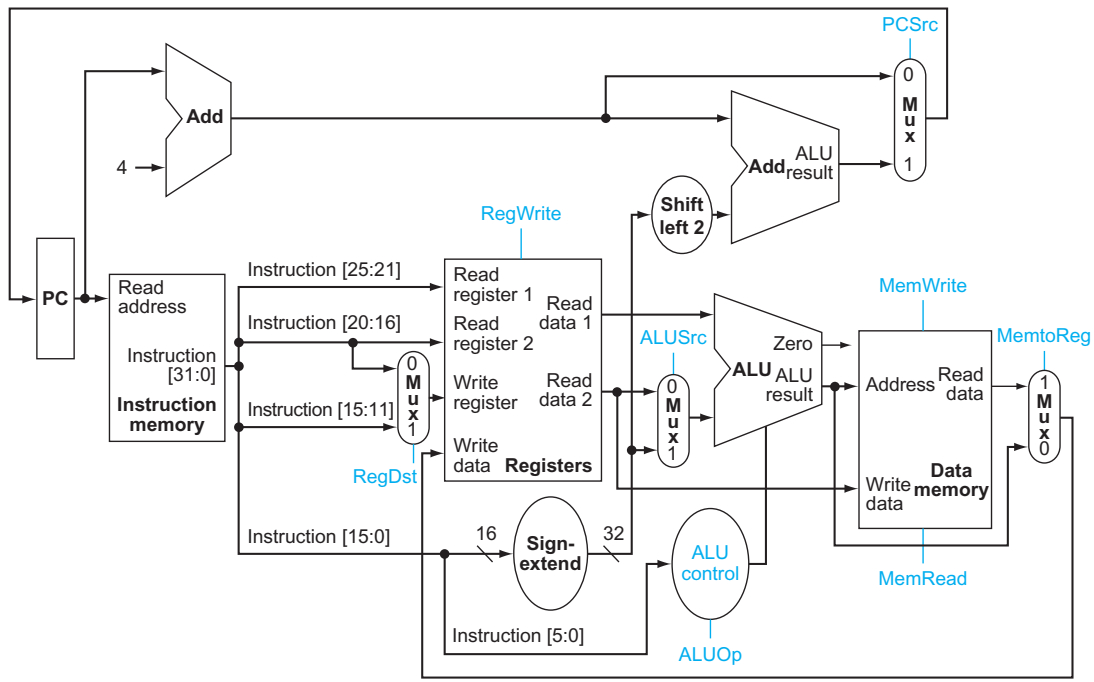

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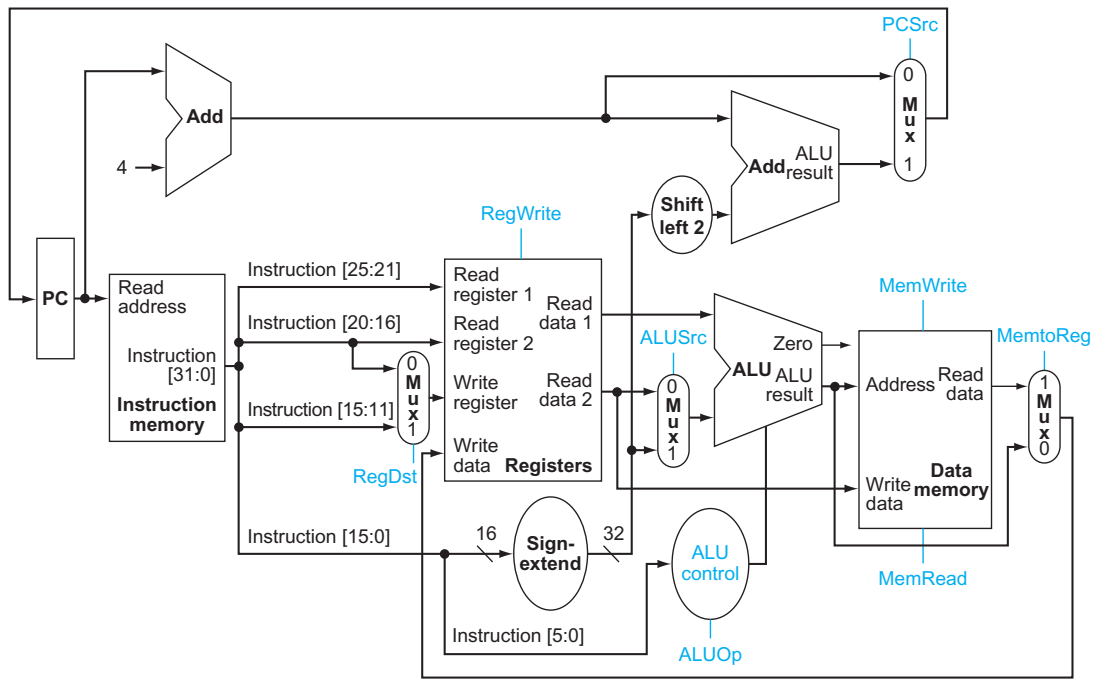

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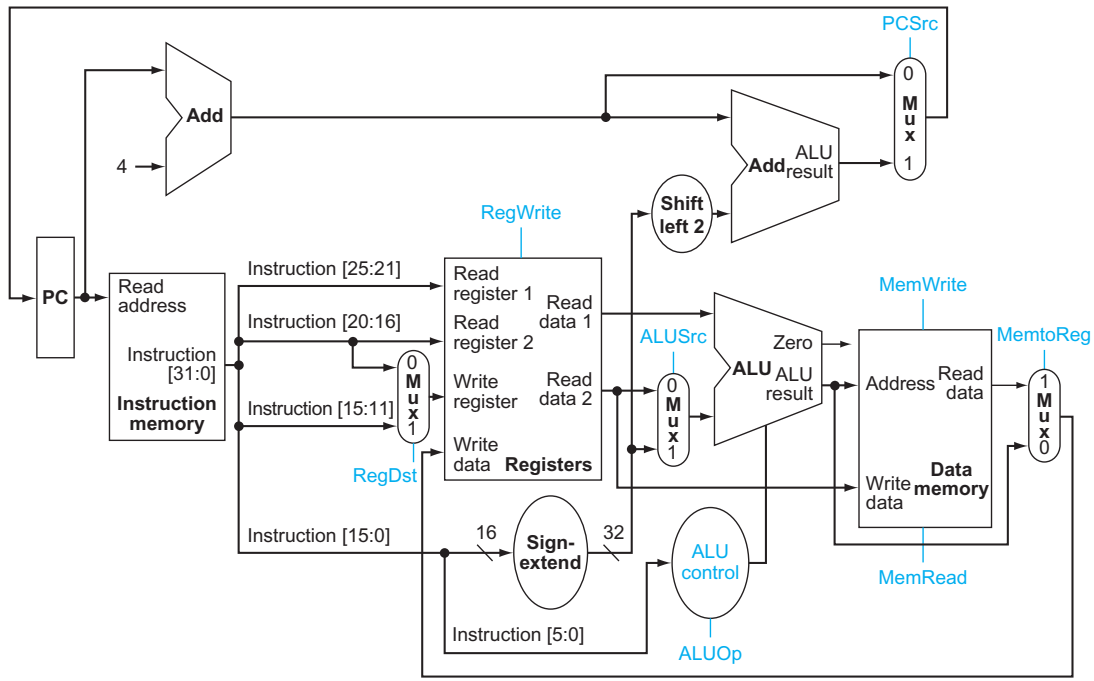

beq rs, rt, address

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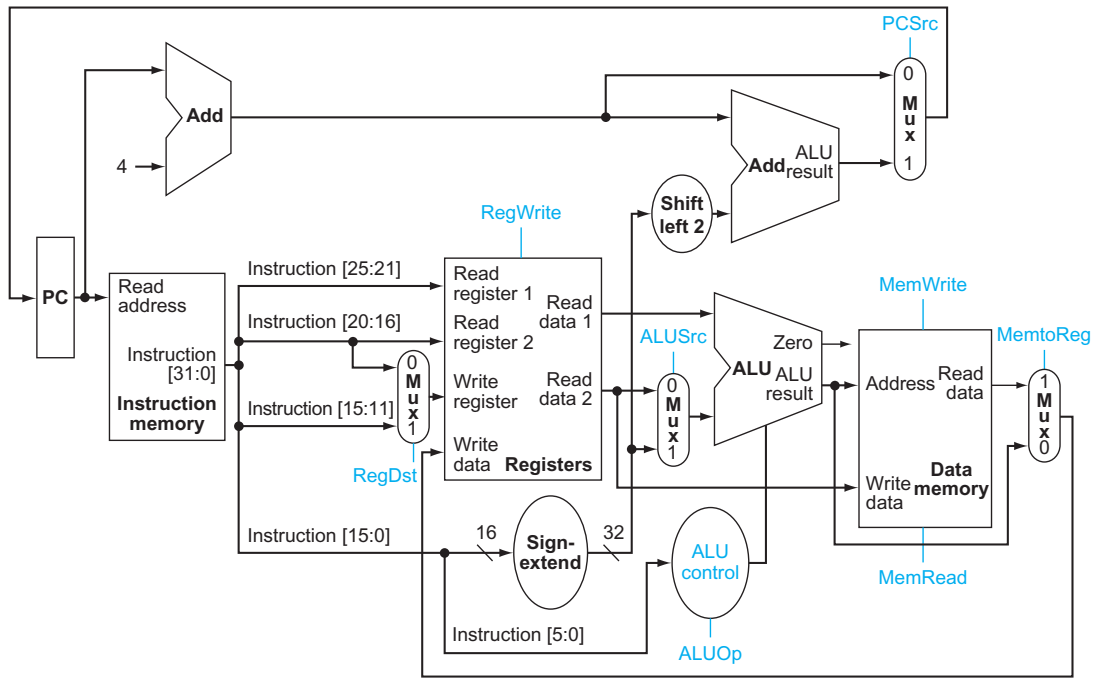

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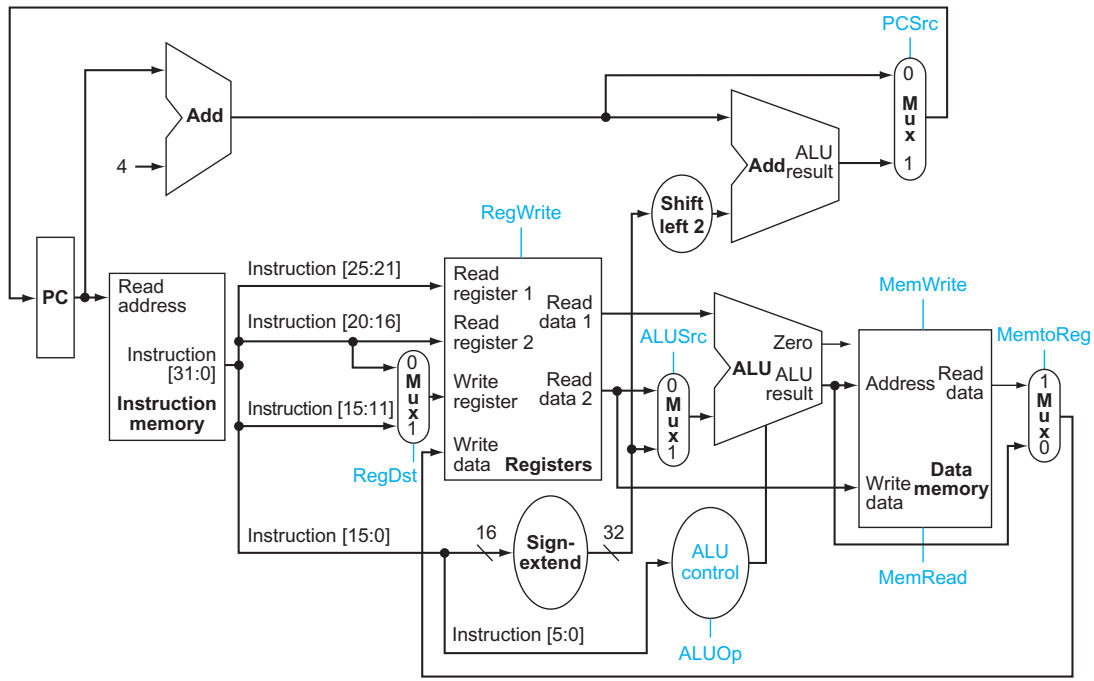

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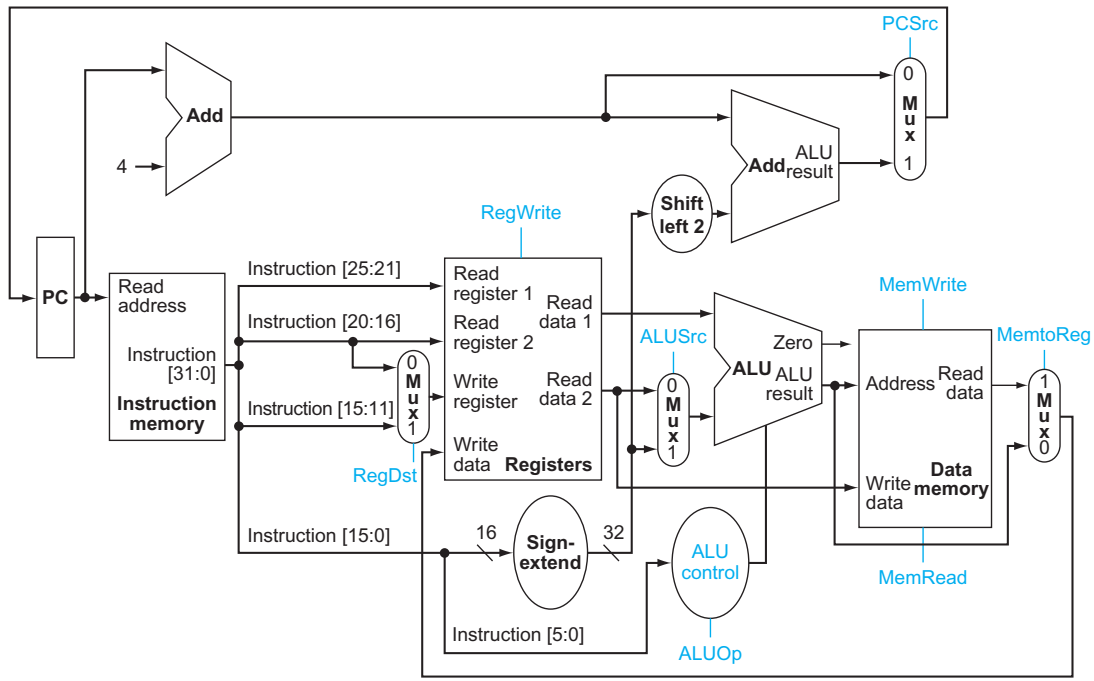

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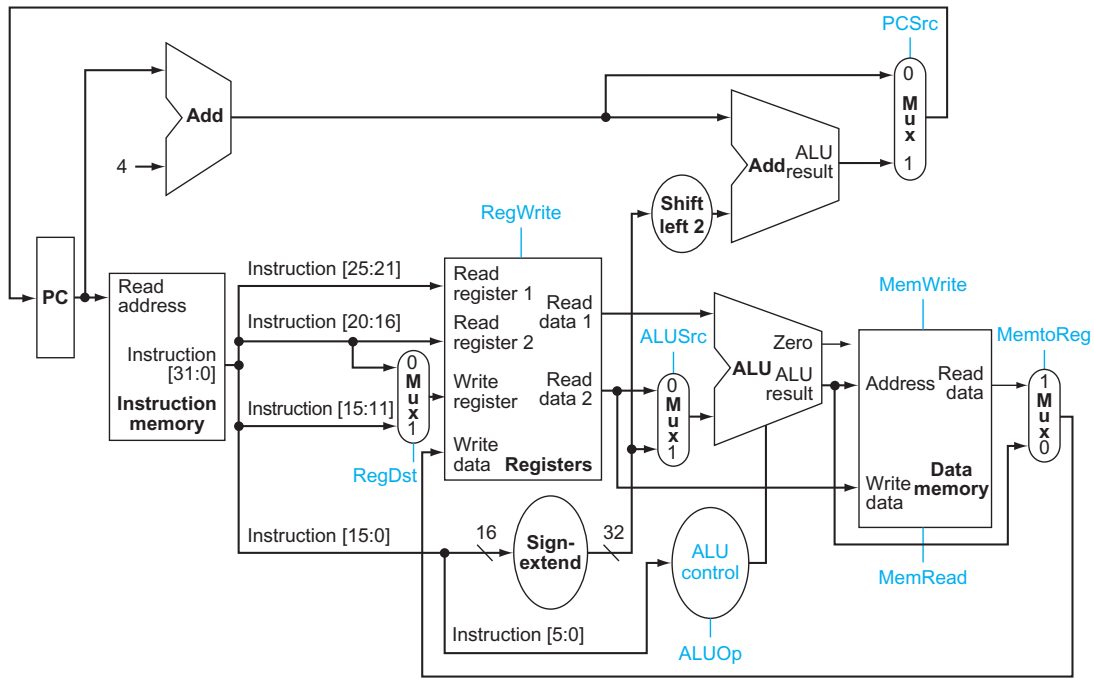

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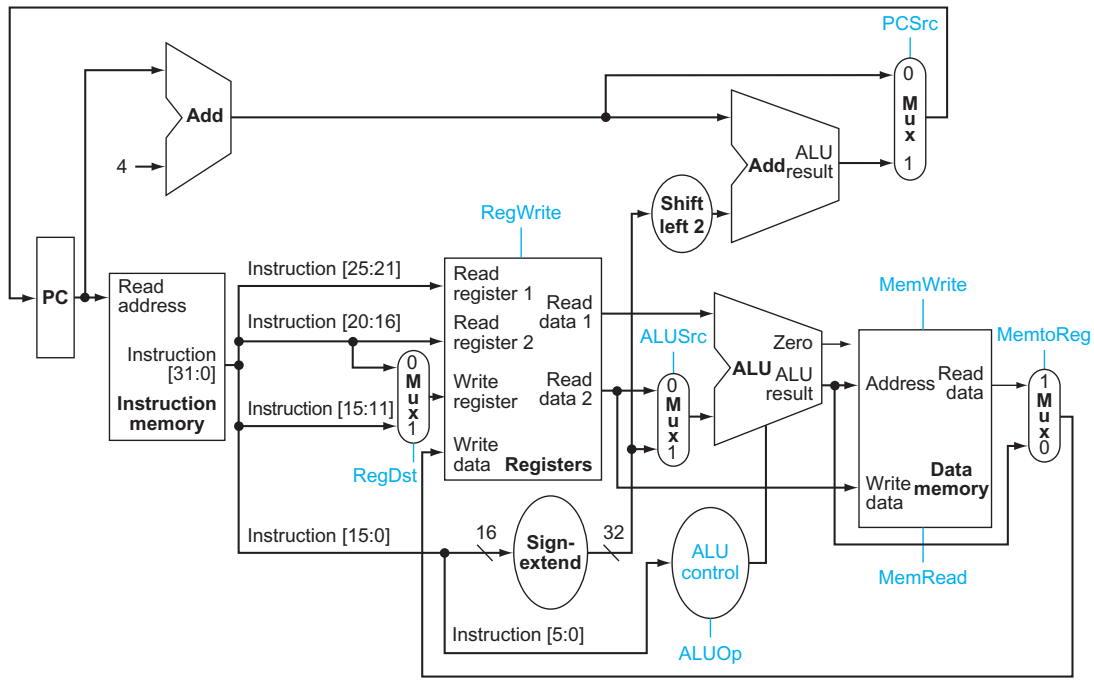
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
PCSrc	PC=PC+4	PC=branch target
MemRead	-	Read data from memory
MemWrite	-	Write data into memory
MemtoReg	Register Write Data from ALU	Register Write Data from data memory



beq rs, rt, address

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	**MemWrite**	MemtoReg
beq	x	0	0	1	0		

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
PCSrc	PC=PC+4	PC=branch target
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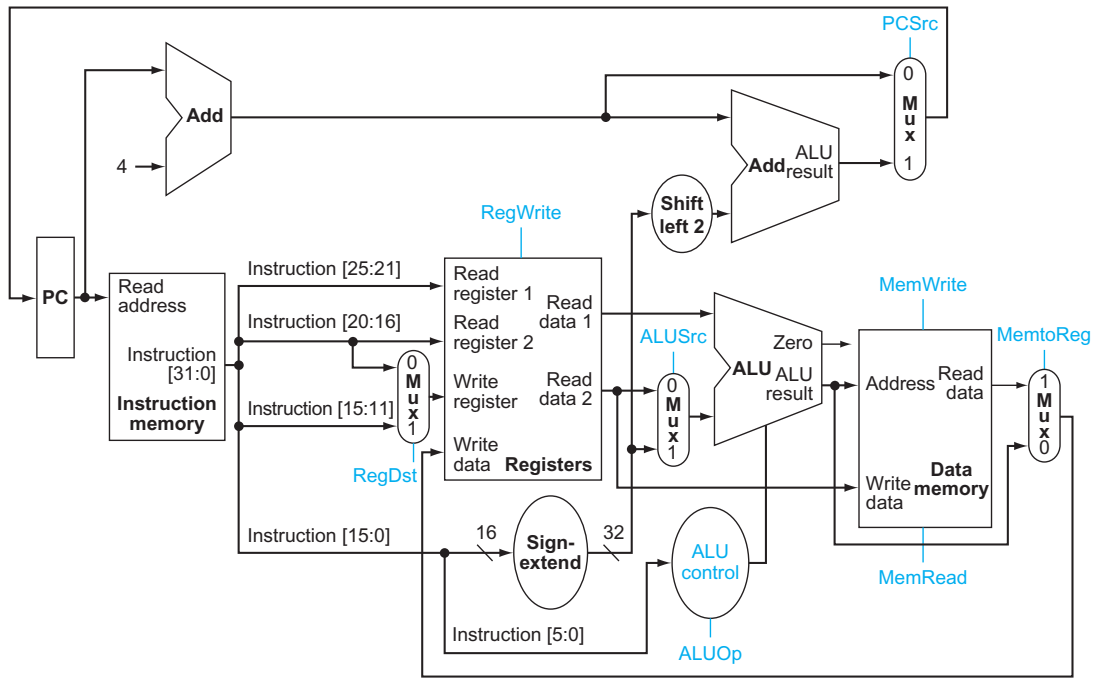

beq rs, rt, address

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	**MemtoReg**
beq	x	0	0	1	0	0	

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
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AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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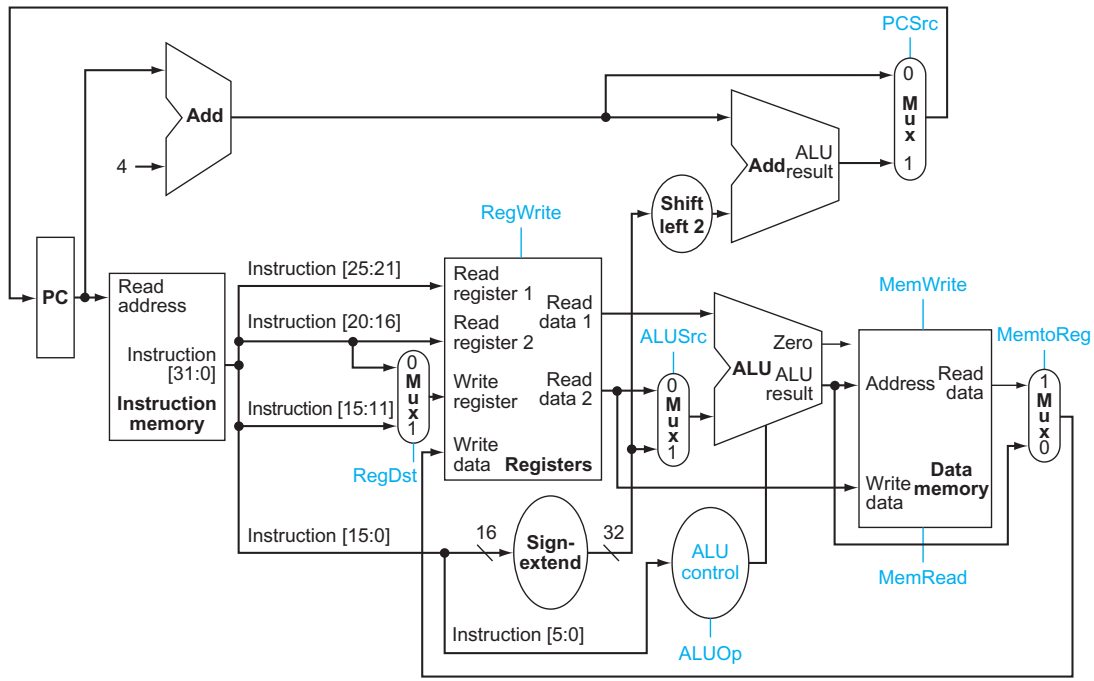
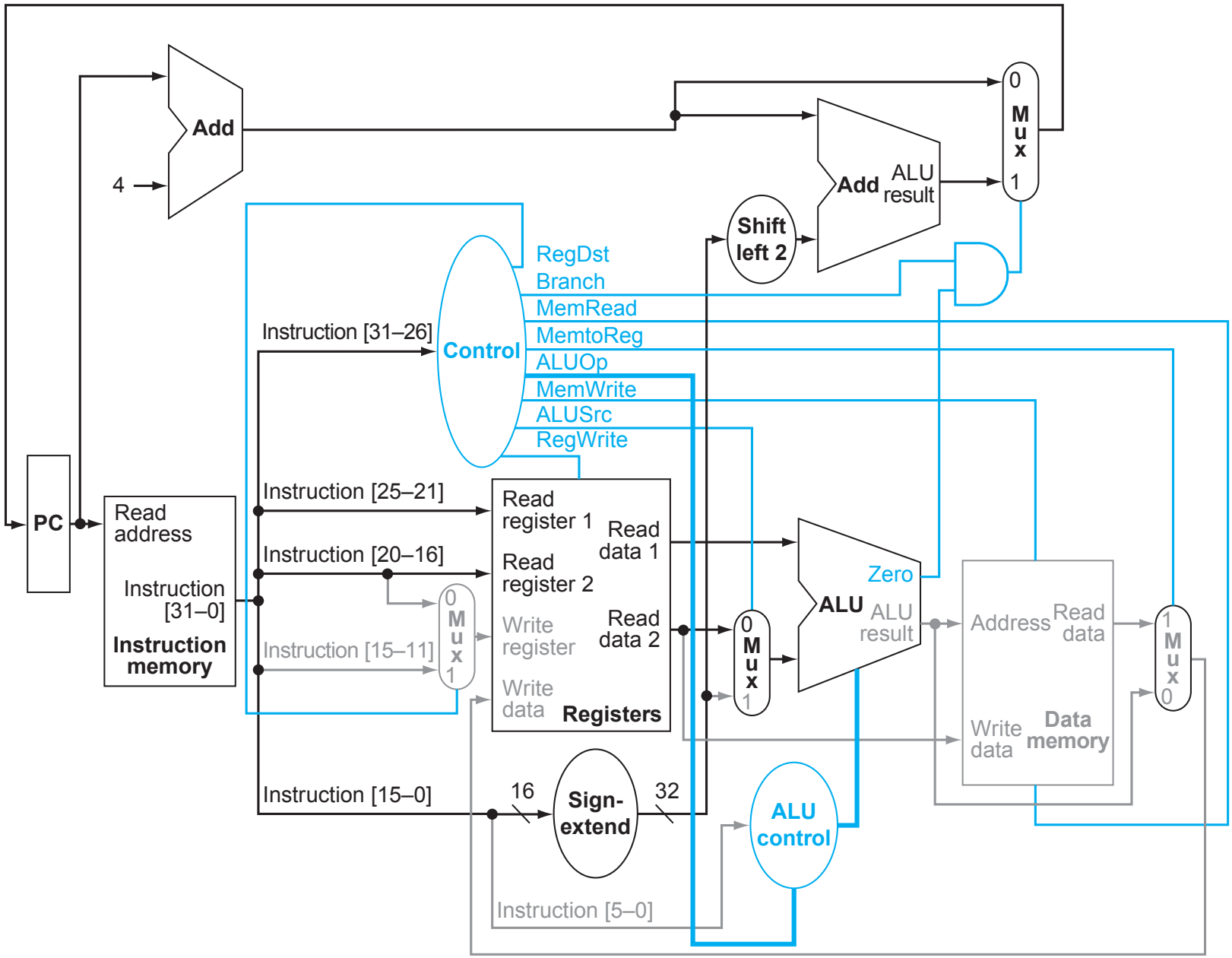


beq rs, rt, address

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
beq	x	0	0	1	0	0	x

beq rs, rt, address



Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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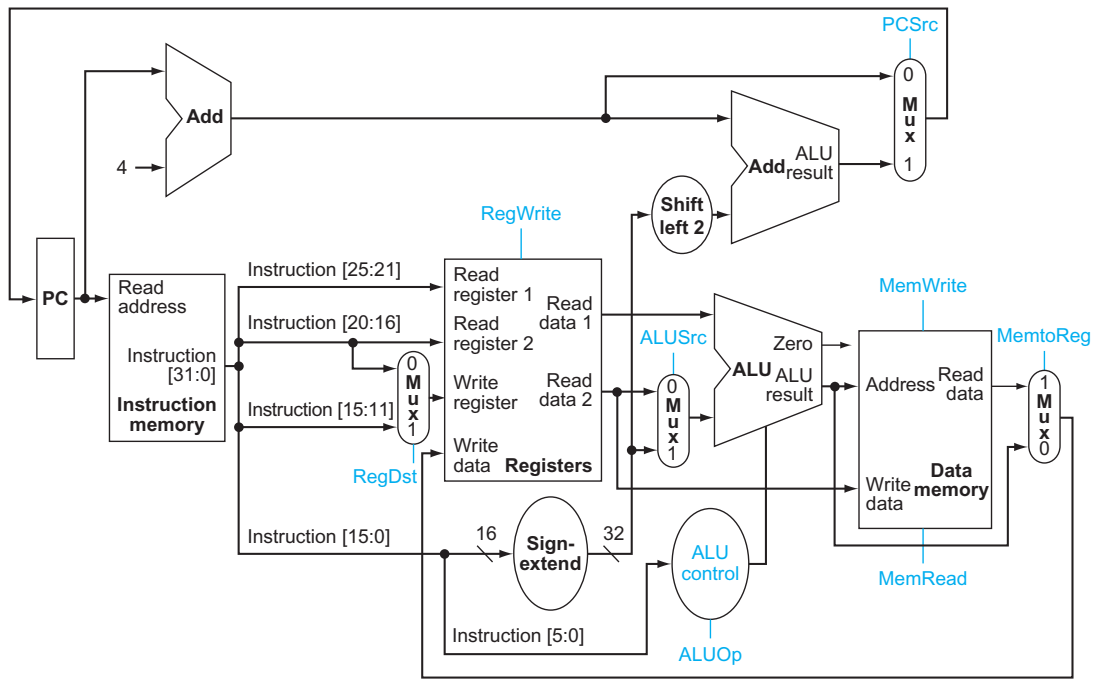

add rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
add							

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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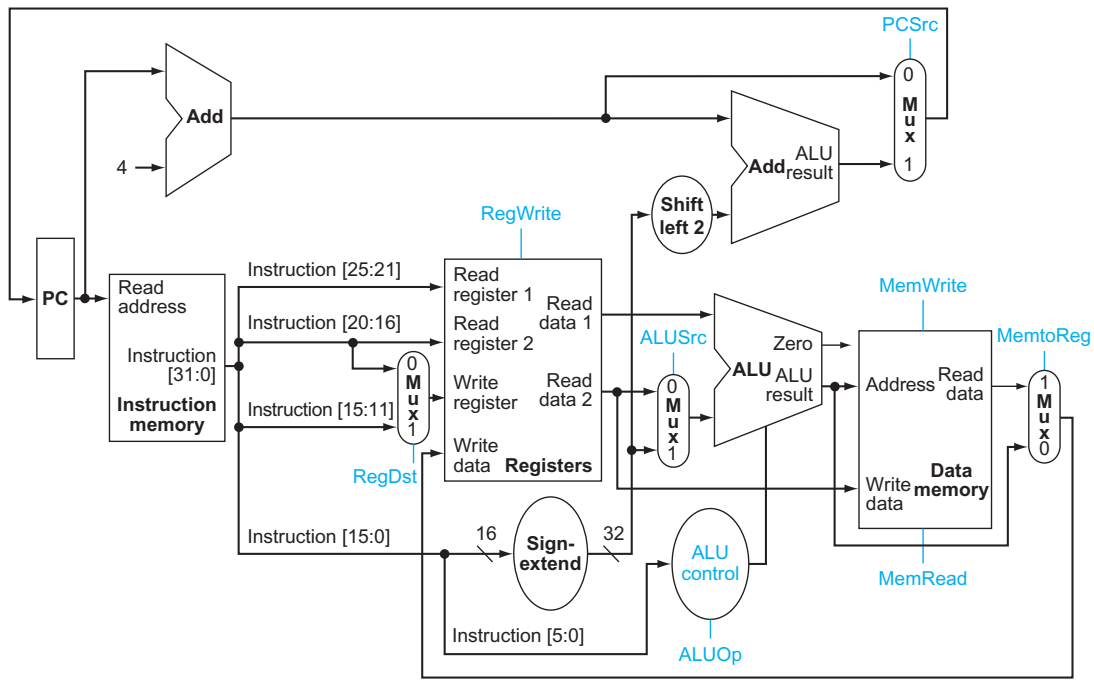

add rd, rs, rt

	RegDst	**RegWrite**	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
add	1						

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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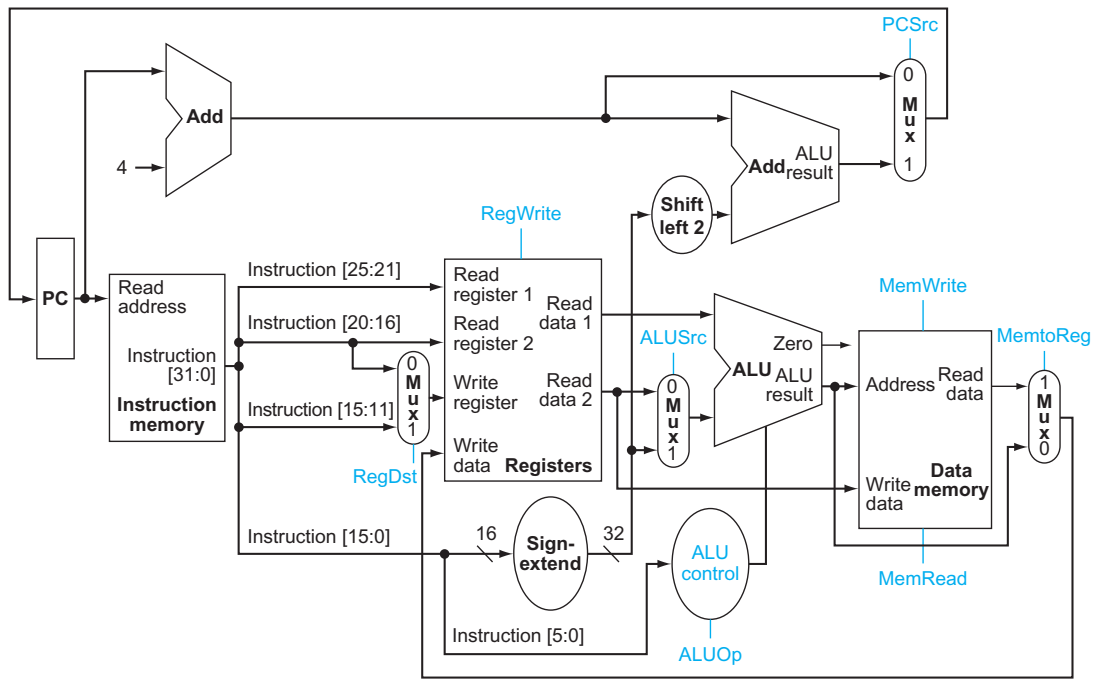

add rd, rs, rt

	RegDst	RegWrite	**ALUSrc**	PCSrc	MemRead	MemWrite	MemtoReg
add	1	1					

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
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AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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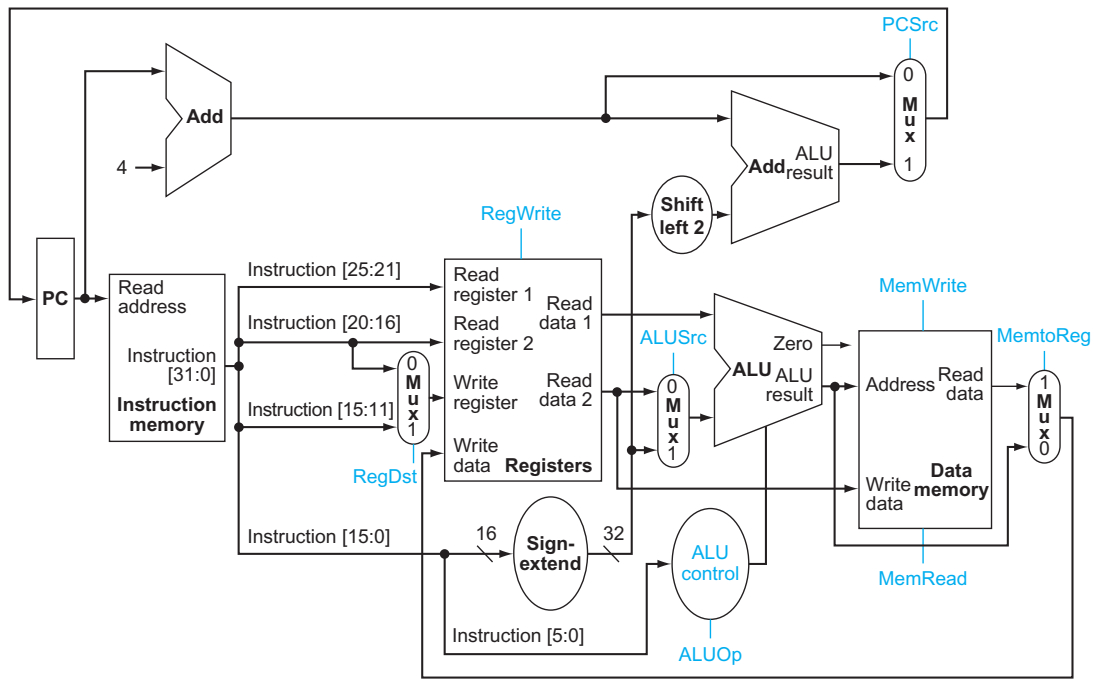

add rd, rs, rt

	RegDst	RegWrite	ALUSrc	**PCSrc**	MemRead	MemWrite	MemtoReg
add	1	1	0				

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
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AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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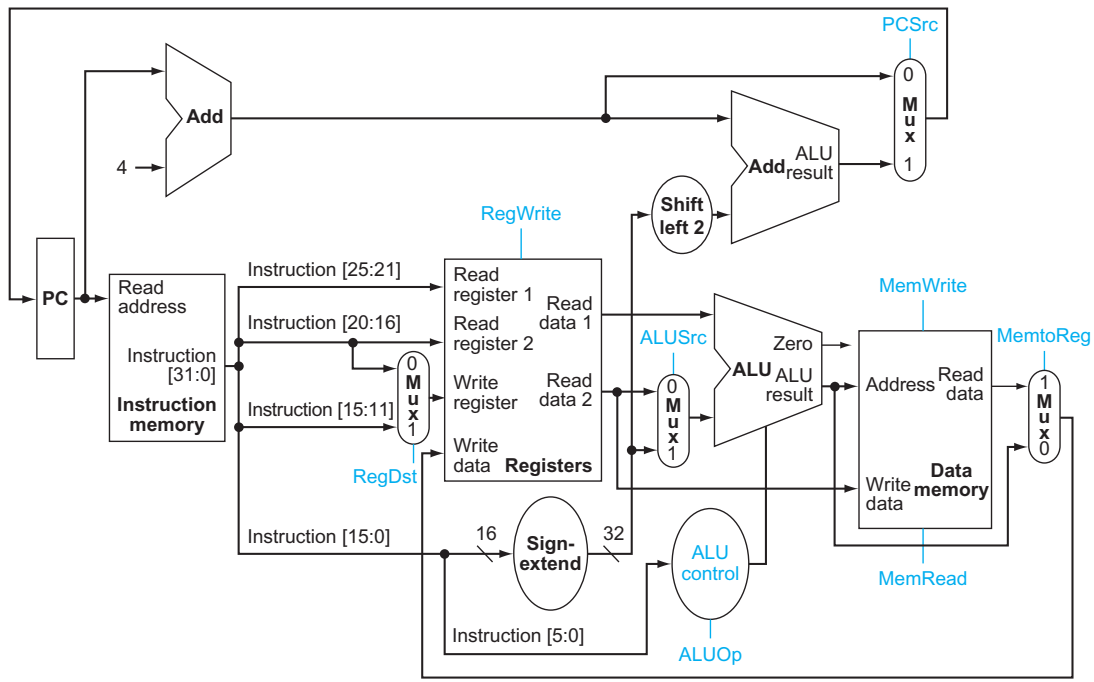

add rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	**MemRead**	MemWrite	MemtoReg
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Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
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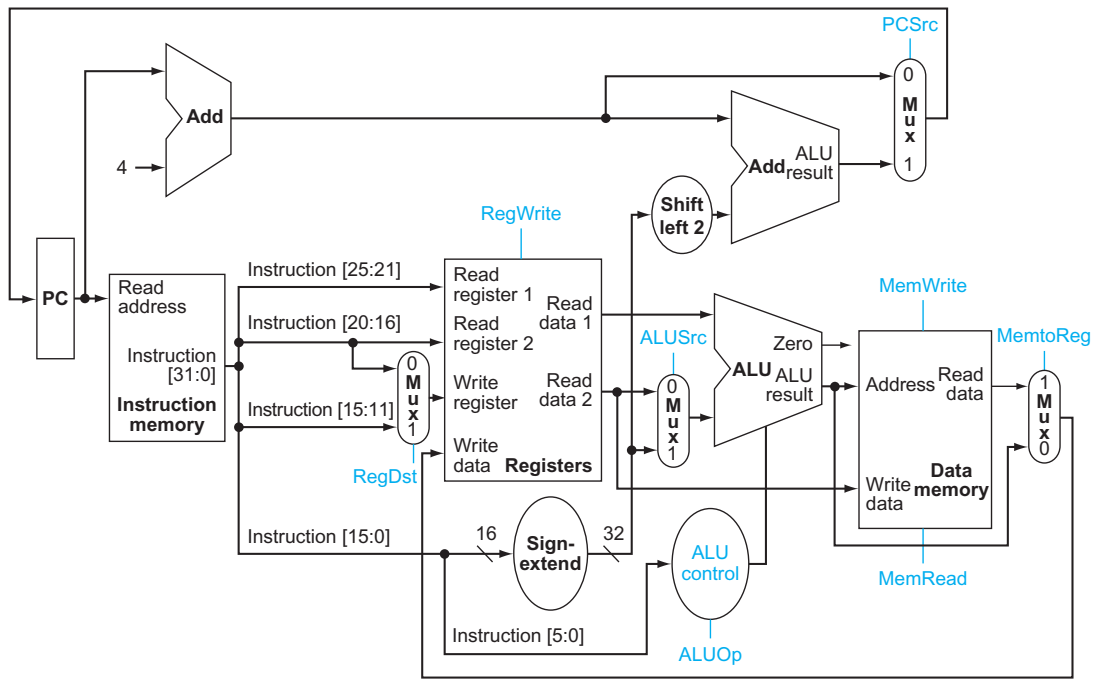

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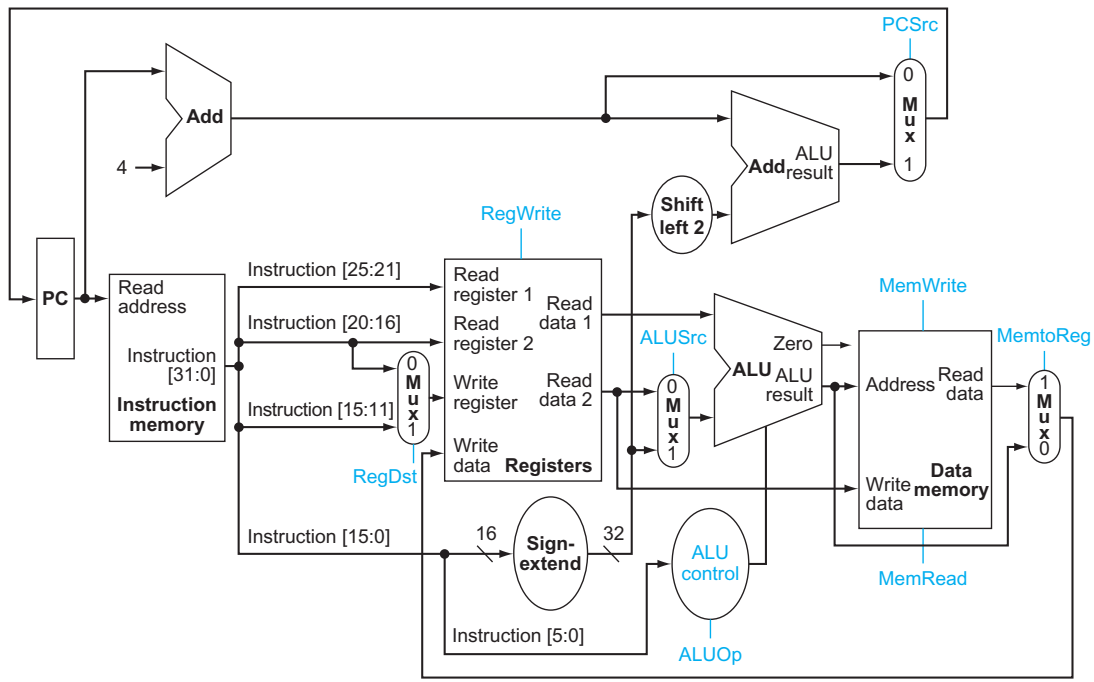

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add	1	1	0	0	0	0	

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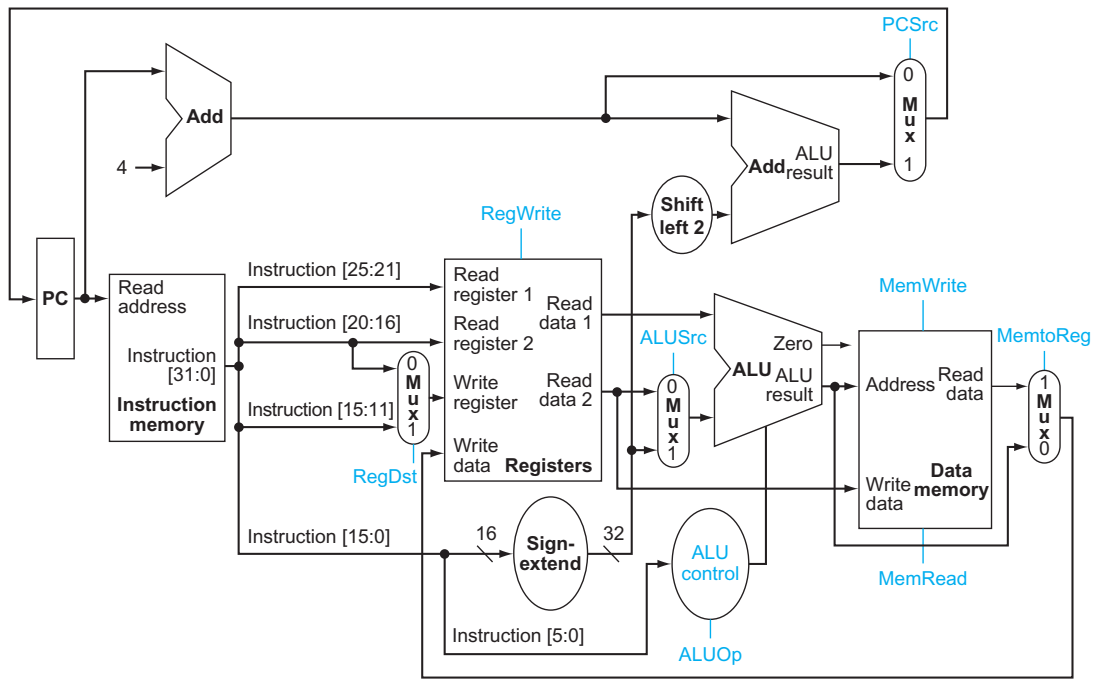

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add	1	1	0	0	0	0	0

Control Signal	0	1
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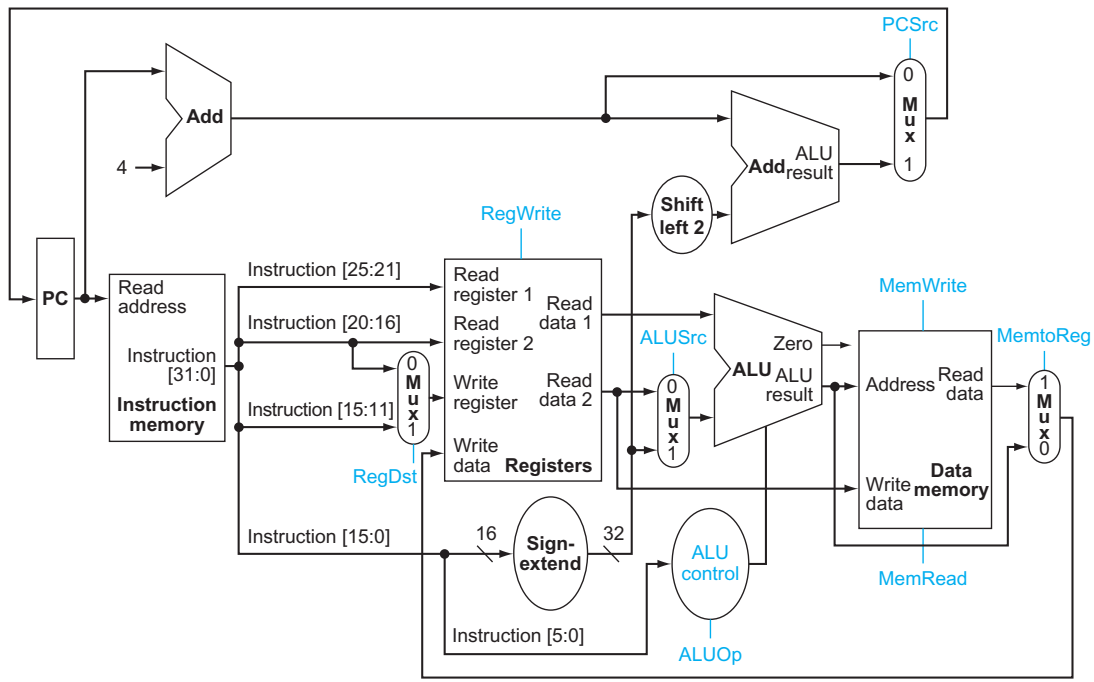

sub rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
sub							

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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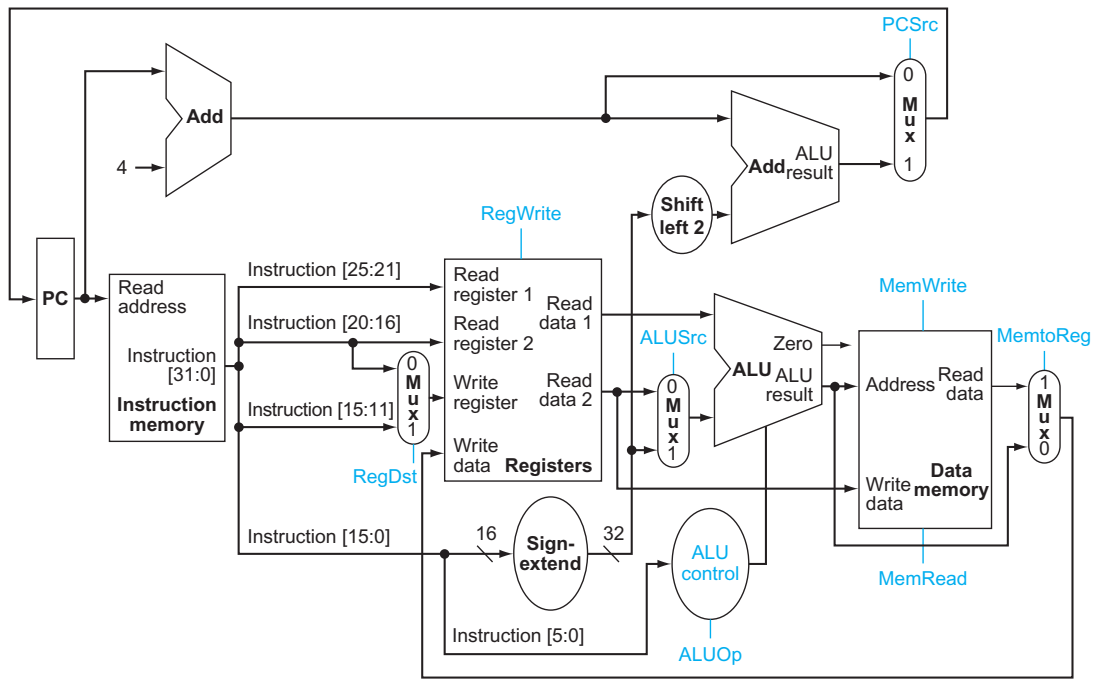

sub rd, rs, rt

	RegDst	**RegWrite**	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
sub	1						

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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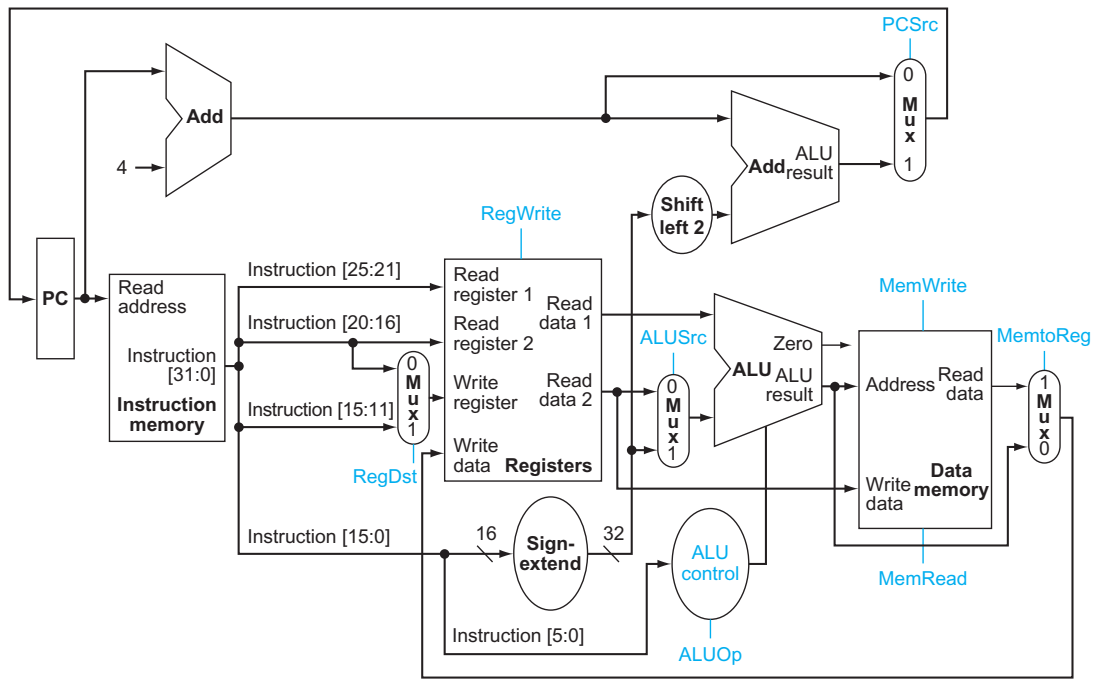

sub rd, rs, rt

	RegDst	RegWrite	**ALUSrc**	PCSrc	MemRead	MemWrite	MemtoReg
sub	1	1					

Control Signal	0	1
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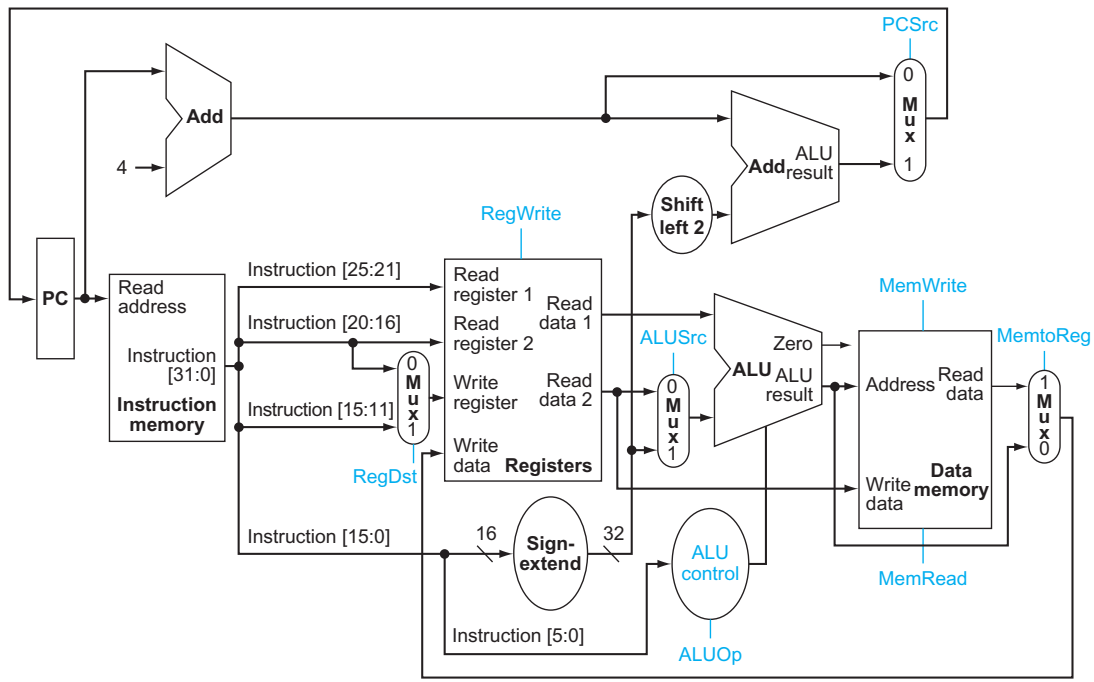

sub rd, rs, rt

	RegDst	RegWrite	ALUSrc	**PCSrc**	MemRead	MemWrite	MemtoReg
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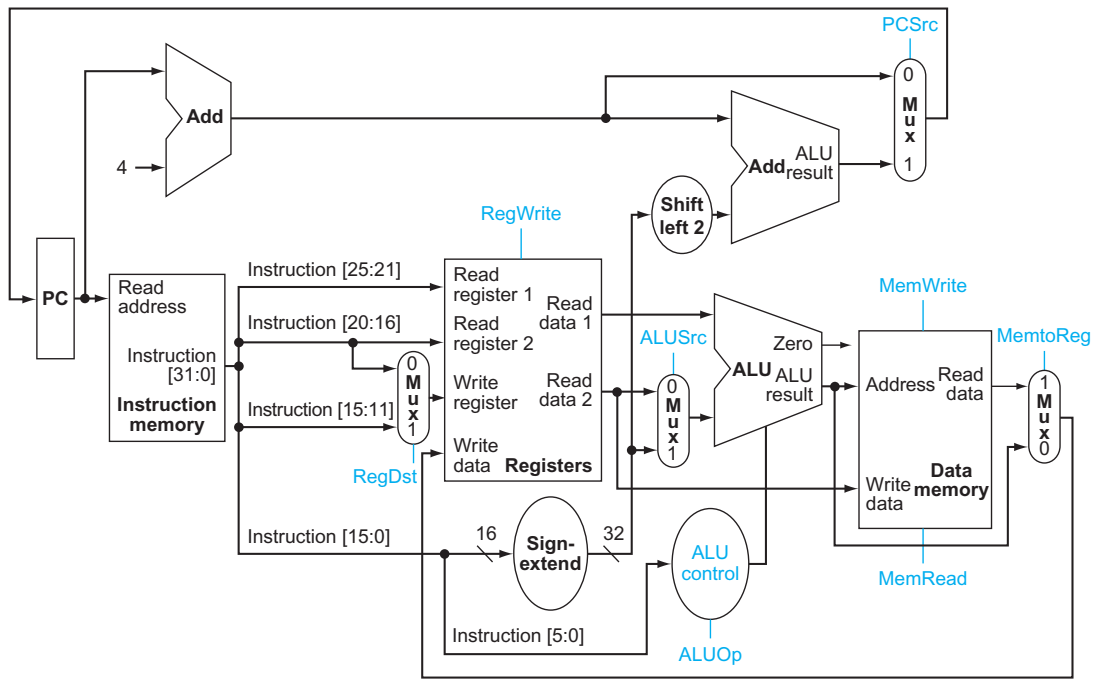

sub rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	**MemRead**	MemWrite	MemtoReg
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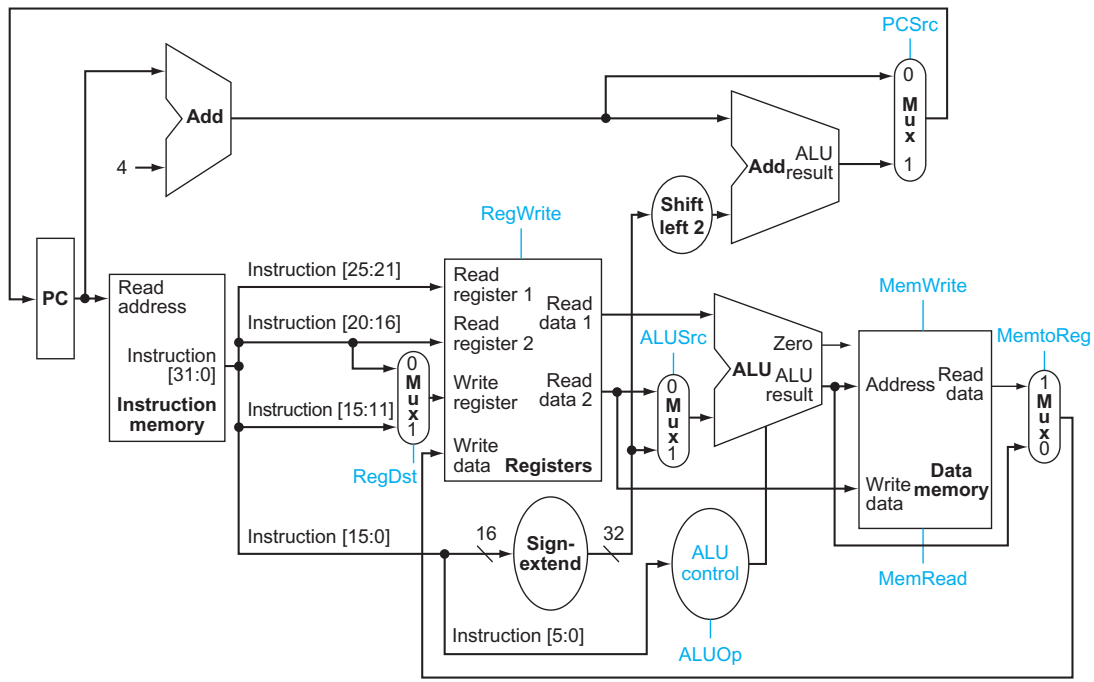

sub rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	**MemWrite**	MemtoReg
sub	1	1	0	0	0		

Control Signal	0	1
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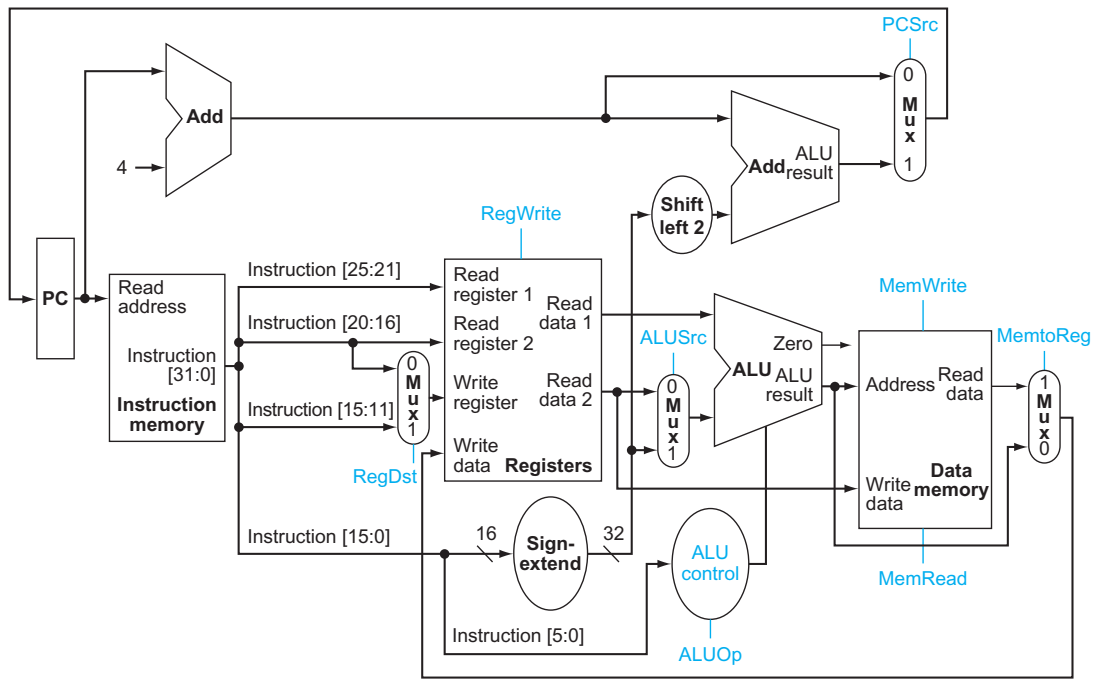

sub rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	**MemtoReg**
sub	1	1	0	0	0	0	

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
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AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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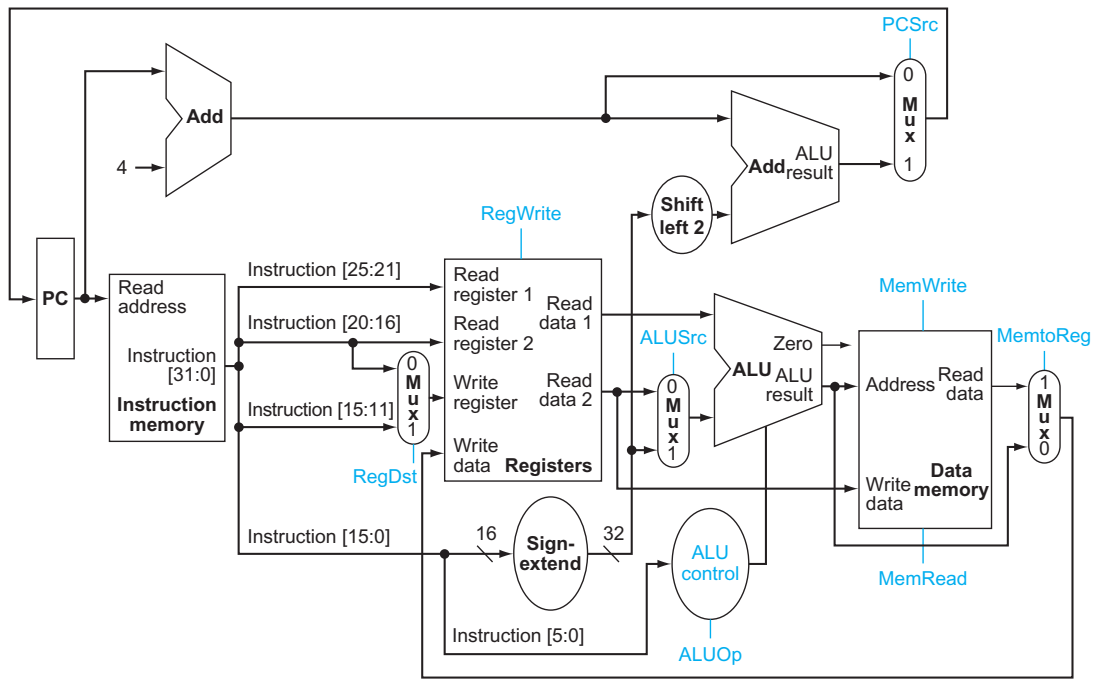

sub rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
sub	1	1	0	0	0	0	0

Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
AluSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
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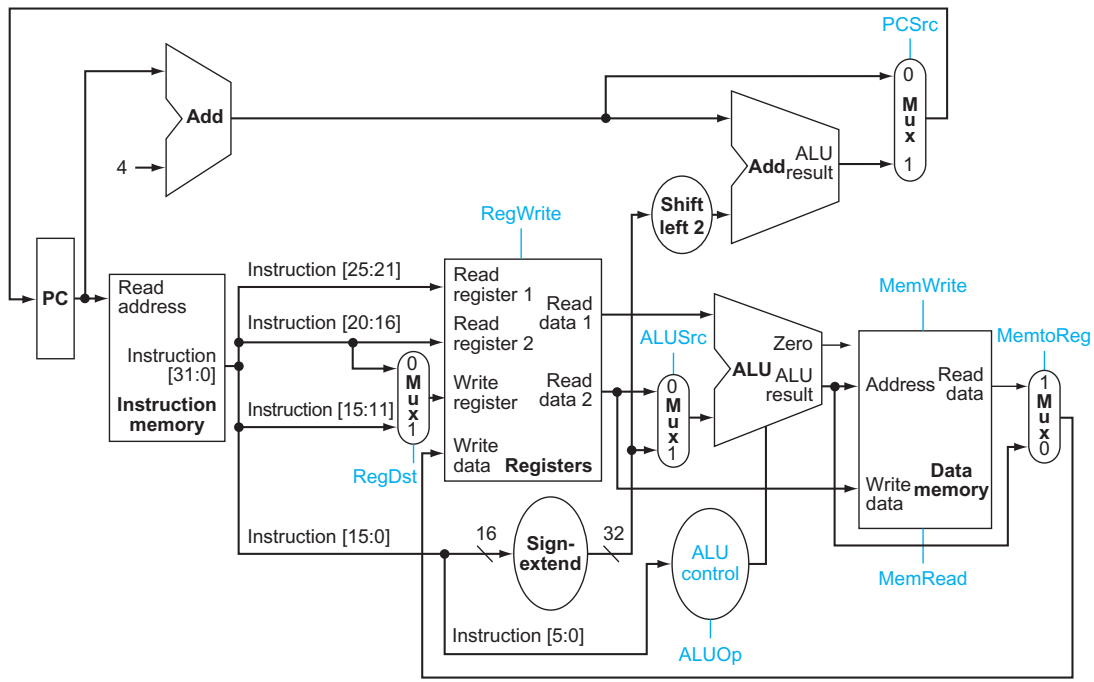
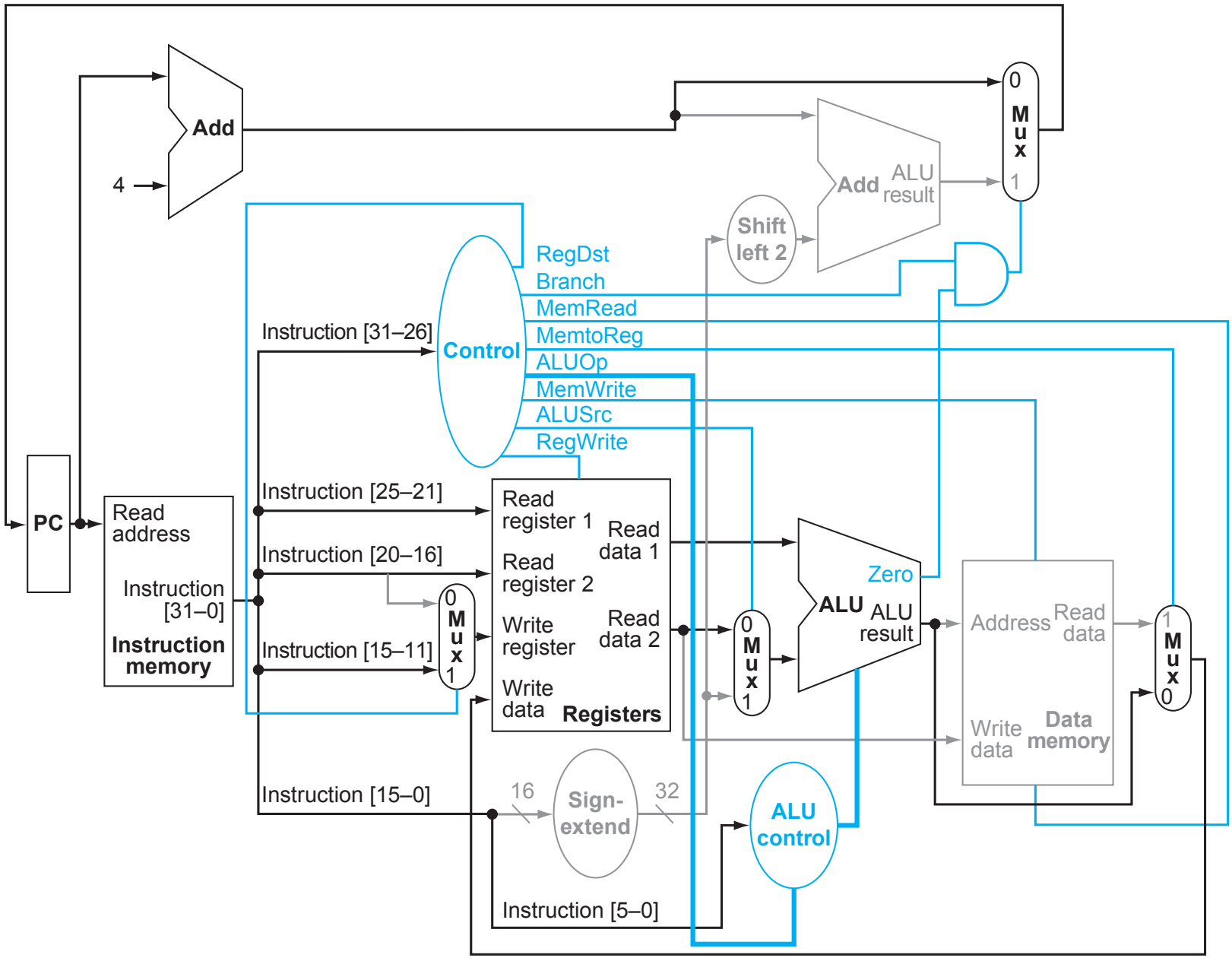


(add/sub/AND/OR/slt) rd, rs, rt

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg
rFormat	1	1	0	0	0	0	0

add rd, rs, rt


Add
4
0
M
u
x
1
Add
ALU result
Shift left 2
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Control
Instruction [31–26]
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
Zero
ALU
ALU result
Address
Read data
Write data
Data memory
16
Sign-extend
32
ALU control

Arithmetic Logic Unit: ALU

ALU Control				Operation
S_3	S_2	S_1	S_0	
0	0	0	0	AND
0	0	0	1	OR
0	0	1	0	ADD
0	1	1	0	SUBTRACT
0	1	1	1	SLT

ALU for different instructions

- `lw rt, 0(rs)` $\leftrightarrow rt \leftarrow [rs+4*0]$,
- `sw rt, x(rs)` $\leftrightarrow [rs+4*x] \leftarrow rt$,
- `beq rs, rt, rd` $\leftrightarrow zero \leftarrow (rs-rt == 0)$
- `add rs, rt, rd` $\leftrightarrow rd = rs+rt$,
- `sub rs, rt, rd` $\leftrightarrow rd = rs-rt$,
- `and rs, rt, rd` $\leftrightarrow rd = rs\&rt$,
- `or rs, rt, rd` $\leftrightarrow rd = rs|rt$,
- `slt rs, rt, rd`,

ALU for different instructions

- `lw rt, 0(rs)` $\leftrightarrow$ $rt \leftarrow [rs + 4 * 0]$, add
- `sw rt, x(rs)` $\leftrightarrow$ $[rs + 4 * x] \leftarrow rt$, add
- `beq rs, rt, rd` $\leftrightarrow$ $zero \leftarrow (rs - rt == 0)$ subtract
- `add rs, rt, rd` $\leftrightarrow$ $rd = rs + rt$, add
- `sub rs, rt, rd` $\leftrightarrow$ $rd = rs - rt$, sub
- `and rs, rt, rd` $\leftrightarrow$ $rd = rs \& rt$, and
- `or rs, rt, rd` $\leftrightarrow$ $rd = rs | rt$, or
- `slt rs, rt, rd`, slt

Decoding Instuctions

	opcode	function
lw	35	-
sw	43	-
beq	4	-
add	0	32
sub	0	34
AND	0	36
OR	0	37
slt	0	42
j	2	-

Decoding Instuctions

Two step Control Unit

	Main Control		function (lsb 6 bit from instruction)						ALU	ALU Control			
	ALUOP1	ALUOP0	F_5	F_4	F_3	F_2	F_1	F_0	operation	S_3	S_2	S_1	S_0
lw	0	0	x	x	x	x	x	x	add	0	0	1	0
sw	0	0	x	x	x	x	x	x	add	0	0	1	0
beq	0	1	x	x	x	x	x	x	sub	0	1	1	0
add	1	x	1	0	0	0	0	0	add	0	0	1	0
sub	1	x	1	0	0	0	1	0	sub	0	1	1	0
AND	1	x	1	0	0	1	0	0	and	0	0	0	0
OR	1	x	1	0	0	1	0	1	or	0	0	0	1
slt	1	x	1	0	1	0	1	0	slt	0	1	1	1

	opcode	function
lw	35	-
sw	43	-
beq	4	-
add	0	32
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ALU Control				Operation
S_3	S_2	S_1	S_0	
0	0	0	0	AND
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0	0	1	0	ADD
0	1	1	0	SUBTRACT
0	1	1	1	SLT

Decoding Instuctions

Two step Control Unit

	Main Control		function (lsb 6 bit from instruction)						ALU	ALU Control			
	ALUOP1	ALUOP0	F_5	F_4	F_3	F_2	F_1	F_0	operation	S_3	S_2	S_1	S_0
lw	0	0	x	x	x	x	x	x	add	0	0	1	0
sw	0	0	x	x	x	x	x	x	add	0	0	1	0
beq	0	1	x	x	x	x	x	x	sub	0	1	1	0
add	1	x	1	0	0	0	0	0	add	0	0	1	0
sub	1	x	1	0	0	0	1	0	sub	0	1	1	0
AND	1	x	1	0	0	1	0	0	and	0	0	0	0
OR	1	x	1	0	0	1	0	1	or	0	0	0	1
slt	1	x	1	0	1	0	1	0	slt	0	1	1	1

	opcode	function
lw	35	-
sw	43	-
beq	4	-
add	0	32
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OR	0	37
slt	0	42
j	2	-

ALU Control				Operation
S_3	S_2	S_1	S_0	
0	0	0	0	AND
0	0	0	1	OR
0	0	1	0	ADD
0	1	1	0	SUBTRACT
0	1	1	1	SLT

Decoding Instuctions

Two step Control Unit

	Main Control		function (lsb 6 bit from instruction)						ALU	ALU Control			
	ALUOP1	ALUOP0	F_5	F_4	F_3	F_2	F_1	F_0	operation	S_3	S_2	S_1	S_0
lw	0	0	x	x	x	x	x	x	add	0	0	1	0
sw	0	0	x	x	x	x	x	x	add	0	0	1	0
beq	0	1	x	x	x	x	x	x	sub	0	1	1	0
add	1	x	1	0	0	0	0	0	add	0	0	1	0
sub	1	x	1	0	0	0	1	0	sub	0	1	1	0
AND	1	x	1	0	0	1	0	0	and	0	0	0	0
OR	1	x	1	0	0	1	0	1	or	0	0	0	1
slt	1	x	1	0	1	0	1	0	slt	0	1	1	1

	opcode	function
lw	35	-
sw	43	-
beq	4	-
add	0	32
sub	0	34
AND	0	36
OR	0	37
slt	0	42
j	2	-

ALU Control				Operation
S_3	S_2	S_1	S_0	
0	0	0	0	AND
0	0	0	1	OR
0	0	1	0	ADD
0	1	1	0	SUBTRACT
0	1	1	1	SLT

Decoding Instuctions

Two step Control Unit

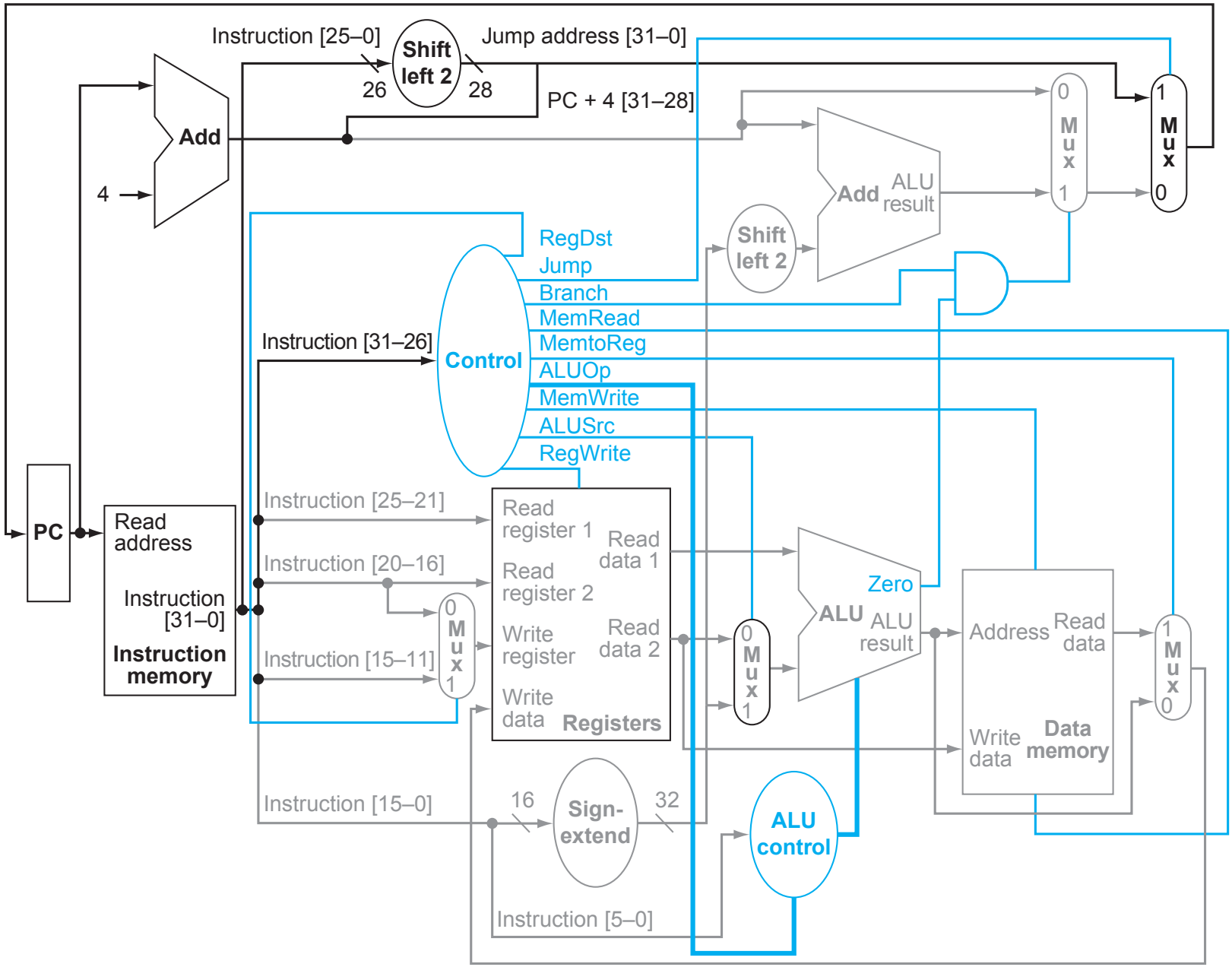
	Main Control		function (lsb 6 bit from instruction)						ALU	ALU Control			
	ALUOP1	ALUOP0	F_5	F_4	F_3	F_2	F_1	F_0	operation	S_3	S_2	S_1	S_0
lw	0	0	x	x	x	x	x	x	add	0	0	1	0
sw	0	0	x	x	x	x	x	x	add	0	0	1	0
beq	0	1	x	x	x	x	x	x	sub	0	1	1	0
add	1	x	1	0	0	0	0	0	add	0	0	1	0
sub	1	x	1	0	0	0	1	0	sub	0	1	1	0
AND	1	x	1	0	0	1	0	0	and	0	0	0	0
OR	1	x	1	0	0	1	0	1	or	0	0	0	1
slt	1	x	1	0	1	0	1	0	slt	0	1	1	1

$$S_3 = 0, S_2 = ALUOP1' ALUOP0 + ALUOP1 F_1, S_2 = \cdots$$

	opcode	function
lw	35	-
sw	43	-
beq	4	-
add	0	32
sub	0	34
AND	0	36
OR	0	37
slt	0	42
j	2	-

ALU Control				Operation
S_3	S_2	S_1	S_0	
0	0	0	0	AND
0	0	0	1	OR
0	0	1	0	ADD
0	1	1	0	SUBTRACT
0	1	1	1	SLT

j address


Instruction [25–0]
Shift left 2
Jump address [31–0]
26
28
PC + 4 [31–28]
Add
4
0
M
u
x
1
1
M
u
x
0
Add
ALU result
Shift left 2
RegDst
Jump
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
ALU
Zero
ALU result
Address
Read data
Write data
Data memory
16
Sign-extend
32
ALU control

j address

	RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg	ALUOP1	ALUOP0	Jump
j	x	x	x	x	x	x	x	x	x	1

Total Main Control Unit

		RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg	ALUOP1	ALUOP0	Jump
R-type	0	1	1	0	0	0	0	0	1	x	0
j	2	x	x	x	x	x	x	x	x	x	1
beq	4	x	0	0	1	0	0	x	0	1	0
lw	35	0	1	1	0	1	0	1	0	0	0
sw	43	x	0	1	0	0	1	x	0	0	0

Total Main Control Unit

		RegDst	RegWrite	ALUSrc	PCSrc	MemRead	MemWrite	MemtoReg	ALUOP1	ALUOP0	Jump
R-type	0	1	1	0	0	0	0	0	1	x	0
j	2	x	x	x	x	x	x	x	x	x	1
beq	4	x	0	0	1	0	0	x	0	1	0
lw	35	0	1	1	0	1	0	1	0	0	0
sw	43	x	0	1	0	0	1	x	0	0	0

$2^6 \times 10$ ROM